VSC Transmission System Using Flying Capacitor Multilevel Converters and Hybrid PWM Control

Lie Xu, *Senior Member, IEEE*, and Vassilios G. Agelidis, *Senior Member, IEEE*

***Abstract*—A high-voltage direct current (HVDC) transmission system based on three-level flying capacitor (FC) multilevel converters with hybrid pulse-width modulation (PWM) is presented in this paper. Selective harmonic elimination PWM (SHE–PWM) is used during normal operating conditions and is switched to phase-shifted sinusoidal PWM (PS–SPWM) during an asymmetric network fault. The generation of the switching patterns under SHE–PWM control for each power device is described taking into account the natural balancing of the FC voltages. A new and simple control method for balancing the FC voltages when using SHE–PWM is proposed which is based on the small change of the firing angle according to the polarity of the load current. The FC voltage ripple under SHE–PWM control is estimated and compared to that under PS–SPWM. A method to implement the proposed hybrid PWM with capacitor voltage balancing is also provided. Simulation studies on a 300-MW/$\pm$150 kV voltage-source converter transmission system are presented to confirm the satisfactory performance of the proposed system under active and reactive power variations and single-phase fault conditions.**

***Index Terms*—Flying capacitor multilevel converter, high-voltage direct current (HVDC), selective harmonic elimination pulse-width modulation (PWM), voltage balancing, voltage-source converter (VSC) transmission.**

I. Introduction

VOLTAGE-SOURCE converter (VSC)-based high-voltage direct current (HVDC) schemes using insulated-gate bipolar transistors (IGBTs) (known as VSC transmission) have attracted increasing attention [1]–[7]. The main advantages of VSC transmission (as schematically shown in Fig. 1), when compared to conventional HVDC systems based on line-commutated thyristor converters, include:

- no requirement for external voltage source for commutation;
- ability to control the reactive power flow independently at each end and independently of the active power control.

However, VSC transmission systems have high-power losses and relatively higher cost when compared to the conventional HVDC system [7]. In order to maximize the potential of VSC transmission systems, a number of technology breakthroughs are required. One requirement is the reduction of the power losses and the harmonic distortion generated by the converters. This will allow the reduction of cooling needs and space requirements as well as increasing the system's operating efficiency and reliability. The other one is to ensure that the system operates satisfactorily during abnormal conditions, such as during severe network unbalances.

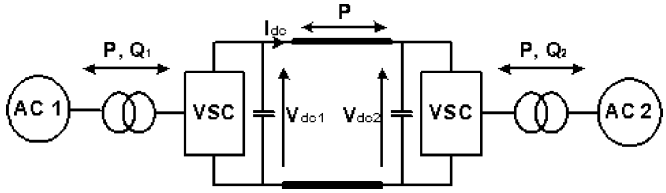

Fig. 1. Basic schematic concept of the VSC transmission system.

Theoretically, one promising way forward could be the adoption of a multilevel converter as a building block for the system. There are a number of distinct multilevel converter topologies which have been used or proposed for the VSC transmission system, namely, the neutral-point clamped (NPC) converter [2], [8], [9], the flying-capacitor (FC) converter [7], [10], and the multimodular converter [3], [4], [11]. While these multilevel converters have their respective merits and shortcomings, the selection of the converter topology is a detailed engineering design exercise [12]. It needs to take into account a number of parameters, including the system design and control, power loss, cost, etc. [12].

Selective harmonic elimination pulse-width modulation (SHE–PWM) allows certain harmonics, usually low-order nontriplen harmonics, to be eliminated by properly selecting the switching instants [13]–[20]. Due to the low equivalent switching frequency and, thus, low switching power loss and good harmonic performance, SHE–PWM has been widely used for high-power applications. However, there is no reported information in the open technical literature on the use of the SHE–PWM for FC converters which are traditionally controlled using phase-shifted sinusoidal PWM (PS–SPWM) [10], [21].

The output phase voltages generated by the SHE–PWM method usually contain triplen harmonics which are then cancelled by the coupling transformer providing the system is balanced. However, during network unbalance, the converters are required to produce three unbalanced outputs [22]. Thus, conventional SHE–PWM cannot be used during unbalanced network conditions since triplen harmonics will not be cancelled under such conditions.

The objective of this paper is to present a study of a VSC transmission system based on three-level FC converters using the proposed hybrid PWM control (i.e., a combination of the SHE–PWM and the PS–SPWM). This paper describes the generation of the switching patterns with SHE–PWM and proposes a method for FC voltage balancing. The impact of such

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L. Xu is with the School of Electronics, Electrical Engineering and Computer Science, Queen's University of Belfast, Belfast BT9 5AH, U.K. (e-mail: l.xu@ee.qub.ac.uk).

V. G. Agelidis is with the School of Engineering Science, Murdoch University, Murdoch 6150, Perth, Australia (e-mail: v.agelidis@murdoch.edu.au).

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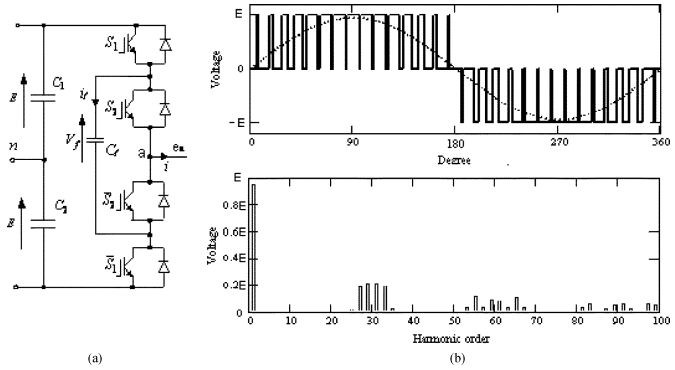


Fig. 2. Three-level FC converter. (a) Single-phase circuit diagram. (b) Phase-to-neutral voltage waveform and harmonic spectrum under PS–SPWM. (Frequency ratio $= 15$, modulation index $M = 0.95$).

a method on FC voltage regulation is described and the circuit for system implementation is illustrated. Furthermore, the FC voltage ripple under the SHE–PWM scheme is estimated. Selected simulation results on a 300-MW/±150-kV system are presented to show the performance of the system.

This paper is organized in the following way. In Section II, the SHE–PWM method for three-level FC converters is discussed. In particular, the way the SHE–PWM switching patterns are generated along with the FC voltage control, the effect of the proposed method on the FC voltage ripple, and the system implementation are analyzed. The proposed hybrid PWM is outlined in Section III. Section IV briefly describes the VSC transmission system modeling and control design. A case study is provided in Section V where simulation results are presented. Finally, conclusions are drawn in Section VI.

II. SHE–PWM for Three-Level FC Converter

A. Principles of FC Converters

Fig. 2(a) shows the schematic diagram of the single-phase leg of a three-level FC converter. C_1 and C_2 are the main dc capacitors and C_f is the FC for phase a. During normal operation, the mean voltages of the FCs for each phase are all charged at E, where the voltage of the main dc bus voltage is $2E$. As a result, the voltage across each switch is only half of the dc-link voltage. Fig. 2(b) shows the typical output phase-voltage waveform and its corresponding harmonic spectrum using PS–SPWM. Two high-frequency triangular carriers are phase-shifted by half the carrier period and the switching patterns are generated by comparing these two carrier waveforms with the modulation signal. The frequency of these carriers, also called the frequency ratio, when normalized to the fundamental frequency of the modulation signal, is chosen to be equal to 15 for the illustrated example (Fig. 2). This arrangement results in the switching frequency for individual switches being the carrier frequency (i.e., 15 p.u.) but the dominant harmonics of the output voltage are positioned around double the carrier frequency and multiples thereof as can be seen from the spectrum shown in Fig. 2(b). This dramatically reduces the switching power losses when compared to a two-level VSC if similar output harmonic distortion is to be achieved. Moreover, if similar power loss is to be maintained, the proposed system requires smaller size filters when compared to a two-level VSC.

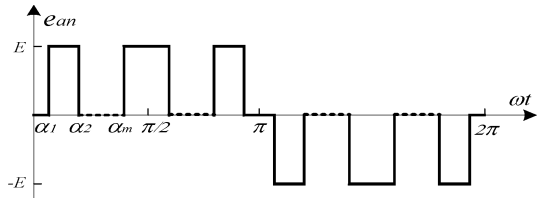


Fig. 3. Phase-voltage waveform of a three-level converter under SHE–PWM control (m switching angles per quarter cycle, main dc voltage is $2E$).

B. SHE–PWM for Three-Level Converters

SHE–PWM for multilevel waveform has been studied in [13]–[20] and only a brief description for three-level waveform is given here. Fig. 3 shows a typical three-level voltage waveform under SHE–PWM control. As can be seen, there are m switching angles within a quarter of the fundamental cycle and the usual quarter-wave and half-wave symmetry of the PWM waveform is retained.

For the waveform shown in Fig. 3, in order to control the fundamental voltage and to eliminate the low order non-triplen harmonics up to the order of $(3m-2)^{\text{th}}$, the following set of equations must be solved:

$$\begin{aligned}
\sum_{i=1}^{m}\left[(-1)^{i+1}\cos(\alpha_i)\right] &= \frac{\pi M}{4}E \\
\sum_{i=1}^{m}\left[(-1)^{i+1}\cos(5\alpha_i)\right] &= 0 \\
&\cdots\cdots \\
\sum_{i=1}^{m}\left[(-1)^{i+1}\cos\left[(3m-2)\,\alpha_i\right]\right] &= 0
\end{aligned} \tag{1}$$

where M is the equivalent modulation index which controls the fundamental output voltage amplitude.

The main challenge associated with the SHE–PWM waveform is to obtain the analytical solutions of the nonlinear transcendental equations given in (1). Many algorithms have been proposed to deal with this problem. They rely either on the starting values to obtain the exact solutions [13]–[16], or introduce a relatively complicated method to ensure convergence and finding all sets of solutions through a sequential homotopy-based computation [17], use of resultant theory, and high-order polynomials [18], and a minimization technique combined with a random search and biased pattern for the initial values applied directly to the set of the transcendental equations [19], [20].

Some general observations for the switching angles solutions of the SHE–PWM method include:

- there are multiple sets of solutions;
- across the entire modulation index range some of these sets of solutions are discontinuous.

As an example, Fig. 4 shows one set of the solutions for nine switching angles per quarter cycle which eliminate nontriplen harmonics up to the 25th included. As can be seen, the solutions discontinue at around the 0.64–0.65 modulation index.

C. SHE–PWM Switching Patterns Generation

For the three-level FC circuit shown in Fig. 2(a), for each phase, the switching patterns for the two outer switches are com-

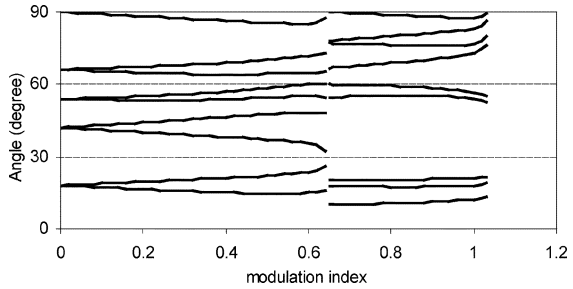


Fig. 4. Calculated firing angles for nine switching angles per quarter cycle (nontriplen harmonics up to the 25th are eliminated).

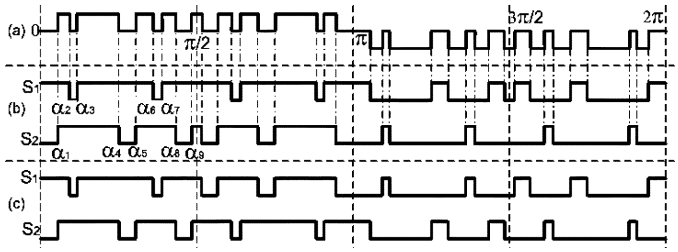


Fig. 5. Generation of the switching patterns. (a) Ideal output three-level phase voltage. (b) Switching pattern I. (c) Switching pattern II.

plimentary and the same applies to the two inner switches. Thus, for the phase-a leg, assuming the FC voltage V_f is E, its output phase-to-neutral voltage can be expressed as

$$e_{an} = E \cdot (S_{P1} + S_{P2} - 1) \tag{2}$$

where S_{P1} and S_{P2} represent the switching states for the switches S_1 and S_2, respectively. S_{P1} and S_{P2} take the value of 1 if the corresponding switch is ON and 0 if the corresponding switch is OFF.

According to the desired output voltage waveform under SHE–PWM control and (2), the switching patterns for the switches can be identified. There are many different combinations of switching patterns which all generate the same output voltage waveform. Taking into account the operation of FC converters, the main criteria for choosing the optimal switching patterns are as follows.

1) The switching stresses for the switches should be kept even. This implies that the number and the distribution of the switching angles for each switch should be similar.
2) Multiple switching (i.e., inner and outer switches switch at the same time, should be avoided).
3) Under ideal conditions, the FC is able to achieve automatic voltage balance within each fundamental frequency cycle for all possible operating modes.

For a voltage waveform of nine switching angles per quarter cycle, Fig. 5 shows two different switching pattern arrangements. It can be seen from Fig. 5 that both switching patterns meet the first and the second criteria and result in a similar switching number for the two switches S_1 and S_2 (i.e., the average switching frequency ratios for S_1 and S_2 are all equal to nine). To achieve similar harmonic performance with PS–SPWM, the switching frequency ratio of 15 is required. This indicates that with SHE–PWM, the switching loss of the FC converter can be reduced substantially if similar harmonic performance is to be retained.

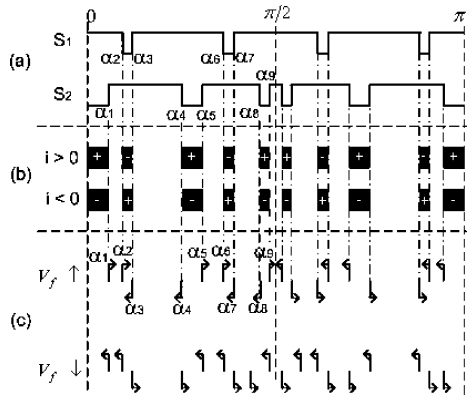


Fig. 6. Effect of the switching angles on the variation of the FC voltages. (a) Switching patterns. (b) Interval during which the FC voltage varies and the direction of the variation: "+" indicates voltage increase and "−" indicates voltage decrease. (c) FC voltage control by slightly modifying the switching angles ($i > 0$) "↑" and "↓" refer to increasing and decreasing FC voltage, respectively; "→" and "←" refer to the increase and decrease of the switching angles, respectively.

To evaluate the impact of the two switching patterns on FC voltage variation (i.e., the third criterion), a program was designed using MathCAD [23]. The program generated the two switching patterns and calculated the corresponding FC voltage variations for all possible operating conditions (i.e., rectifier, inverter, purely capacitive, and purely inductive load conditions). It has been found that with switching pattern I, for each of the four operational modes, the FC voltage at the end of each fundamental period goes back to the value it started at the beginning of that period. This indicates that the FC voltage is automatically balanced under ideal conditions with switching pattern I. However, with switching pattern II, when the converter operates at purely inductive or capacitive mode, the FC voltage cannot achieve automatic balance. Thus, switching pattern II does not meet the third criterion and cannot be used. For any other output voltage waveforms with a different number of switching angles, the same principles can also be applied to find the optimal switching patterns.

D. FC Voltage Control

In a practical system, the control signals could have a slightly different duty cycle, the power devices have different characteristics, and the load current may be temporary asymmetrical. Consequently, the voltages of the FC can vary even with switching pattern I. Therefore, appropriate methods must be integrated in the control to ensure the balance of the FC voltages.

The current flowing into the FC i_f can be expressed using the switching states of the power devices as

$$i_f = i \cdot (S_{P1} - S_{P2}) \tag{3}$$

where i is the output phase current.

According to (3), the voltage variations of the FC within each switching period can be synthesized and the results are shown in Fig. 6 for half a fundamental period. Specifically, Fig. 6(a)

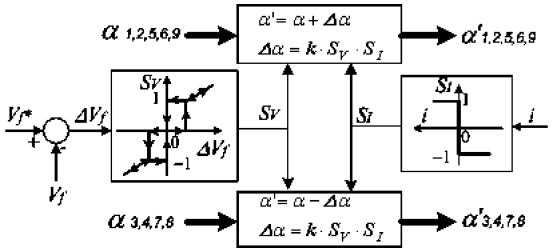


Fig. 7. Schematic diagram of the proposed capacitor voltage-control method.

shows the switching patterns and Fig. 6(b) shows the variations of the FC voltage for different phase current polarities. During the intervals which are marked black in the figure, the FC voltage varies according to the sign indicated. As the average FC voltage is determined by its charging and discharging energy, in order to control the FC voltage, the switching angles are thus slightly modified to change the average charging and discharging times of the FC within each fundamental period. For example, assuming the output phase current is positive (i.e., $i > 0$), if the average FC voltage is too low and needs to be increased, the firing angles of α_1, α_2, α_5, α_6, and α_9 are slightly increased while α_3, α_4, α_7, and α_8 are slightly decreased. As schematically illustrated in Fig. 6(c), this causes the charging time of the FC to increase and the discharging time to decrease and, consequently, the average FC voltage increases. The opposite actions apply if V_f needs to decrease or the output phase current i is negative. The changes of the switching angles are usually very small such that good harmonic performance of the SHE–PWM waveform is maintained.

The capacitor voltage regulation under such a control method can be estimated by considering the changes of the charging and discharging times. Assume the change of the switching angle is $\Delta\alpha$ (degree) and the phase current is $i = I_m \sin(\omega_s t - \varphi)$, the change of the capacitor charge within half the fundamental cycle ($\omega_s t = \varphi$ to $\pi + \varphi$) for SHE–PWM with m switching angles per quarter cycle is given by

$$\begin{aligned}\Delta Q_f = &\frac{\Delta\alpha}{360} T_1 I_m \left[\sum_{i=k+1}^{m} \sin(\alpha_i - \varphi) + \sum_{i=1}^{m} \sin(\pi - \alpha_i - \varphi) \right. \\ &\left. + \sum_{i=1}^{k} \sin(\pi + \alpha_i - \varphi) \right] \\ = &\frac{\Delta\alpha}{360} T_1 I_m \left[\left| \sum_{i=1}^{m} \sin(\alpha_i - \varphi) \right| + \sum_{i=1}^{m} \sin(\alpha_i + \varphi) \right] \quad (4a)\end{aligned}$$

where $\alpha_k < \varphi < \alpha_{k+1}$ and T_1 is the fundamental period. Thus, the FC voltage change with one fundamental period is given by

$$\Delta V_f = \frac{\Delta\alpha}{180 C_f} T_1 I_m \left[\left| \sum_{i=1}^{m} \sin(\alpha_i - \varphi) \right| + \sum_{i=1}^{m} \sin(\alpha_i + \varphi) \right]. \quad (4b)$$

Fig. 7 shows the schematic diagram of the proposed FC voltage control scheme. For a three-phase converter, three such controllers are required, one for each phase. The phase current is measured and its polarity S_I is determined. The error of the FC voltage is also calculated and passed into a hysteresis controller, which generates the FC voltage status S_V. The firing angles are then modified according to S_I and S_V as shown in Fig. 7. The constant k, shown in Fig. 7, is normally very small (i.e., in the range of 0.1–0.2 of a degree so that the benefits of good harmonic characteristics of the SHE–PWM method are not affected). As can be seen, large voltage error generates a larger value of S_V and results in larger switching angle changes which indeed provides faster voltage correction. This is especially useful during or immediately after transients as the system can provide fast voltage balancing to minimize the stresses on the power devices. The harmonic distortion may temporarily increase during such conditions. However, this may not be a concern under transient conditions.

E. FC Voltage Ripple Estimation

As can be seen from Fig. 6, if the longest FC charging or discharging period coincides with the peak of the phase current, it results in the maximum FC voltage ripple. Furthermore, Fig. 6 also shows that within the converter operating range, at phase angles close to 0 and π, two consecutive FC voltage changes can have the same direction for a long period (large α_1 as seen from Fig. 3). Therefore, maximum FC voltage ripple is generated if the ac current is around its maximum value at 0 or π (i.e., purely inductive or capacitive operation). The maximum FC voltage ripple with SHE–PWM can then be estimated for this specific switching angle arrangement as

$$\Delta V_{f(\mathrm{SHE-PWM})} = \frac{1}{C_f} \int i dt \approx \frac{1}{C_f} I_m \frac{2\alpha_1}{360} T_1 = \frac{I_m \cdot \alpha_1 \cdot T_1}{180 C_f}. \quad (5)$$

For comparison, the maximum FC voltage ripple under PS–SPWM control is also generated under purely inductive or capacitive mode and it is given by

$$\Delta V_{f(\mathrm{PS-SPWM})} = \frac{1}{C_f} \int i dt \approx \frac{1}{C_f} I_m \frac{T_{sw}}{2} \quad (6)$$

where T_{sw} is the period of the carrier frequency.

Thus, the ratio of the FC voltage ripples between the two alternative PWM methods is given as

$$\frac{\Delta V_{f(\mathrm{SHE-PWM})}}{\Delta V_{f(\mathrm{PS-PWM})}} = \frac{\alpha_1}{90} \cdot \frac{T_1}{T_{sw}} = N \cdot \frac{\alpha_1}{90} \quad (7)$$

where N is the frequency ratio.

As described in previous sections, the equivalent switching frequency ratio for SHE–PWM with nine angles per quarter cycle is nine. For PS–SPWM with the same switching frequency ratio, (7) indicates the ratio of the FC voltage ripple between the two PWM methods is 1.23 at $M = 1.0$ where the maximum α_1 is 12.3°. If the frequency ratio of 15 were used for PS–SPWM to achieve similar harmonic performance as SHE–PWM, (7) would give a value of 2.05.

F. System Realization

A possible way for implementing the proposed SHE–PWM method is schematically shown in Fig. 8. It involves the generation of a triangular reference waveform, which has the same frequency and phase shift as the desired converter ac voltage output. For a three-phase system, three triangular reference waveforms are needed with each phase shifted by 120°. According to the desired modulation index M from

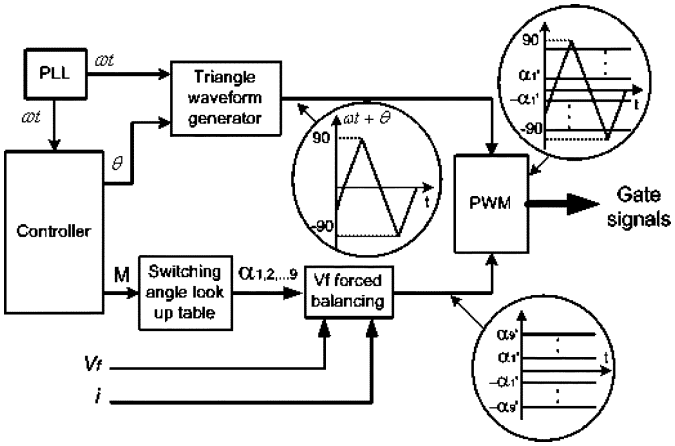


Fig. 8. Schematic diagram of the implementation of SHE–PWM for the three-level FC converter with FC voltage forced balancing (nine angles per quarter cycle).

the controller output, the switching angles are fetched from the lookup table. Taking into account the requirement of FC voltage balancing control, a number of switching thresholds (i.e., $\alpha_1^*, \alpha_2^*, \ldots \alpha_9^*, -\alpha_1^*, -\alpha_2^*, \ldots -\alpha_9^*$) are generated. They are then compared to the triangular reference waveforms to generate the switching signals for the power devices.

III. Proposed Hybrid PWM

Under normal operation, the three-phase ac system is balanced (or with very little unbalance) and, therefore, the three-phase output voltages from the converter are also balanced. Consequently, triplen harmonics contained in the converter output voltages with SHE–PWM control are cancelled by the delta or open star-connected transformer secondary windings. However, during severe ac system unbalanced conditions, especially during an asymmetrical fault, in order to control the system properly, the converter is required to output unbalanced three-phase voltages [22]. If the same SHE–PWM method were used, large triplen harmonics would appear on the network side, as they could not be completely cancelled by the transformer.

On the other hand, the commonly used PS–SPWM automatically suppresses all low-order harmonics including the triplen ones and, thus, can be used for generating the pulses under unbalanced condition. The FC voltages under PS–SPWM can also be fully controlled by control actions even under transient conditions [24]. To combine the advantages of both SHE–PWM and PS–SPWM, the use of a hybrid PWM scheme for VSC transmission systems based on the FC converter is proposed in this paper (i.e., the SHE–PWM is used under normal operating conditions and this is switched to PS–SPWM under unbalanced conditions). The carrier frequency when switched to PS–SPWM is selected such that the lowest dominant harmonic frequencies under PS–SPWM are similar to that of SHE–PWM. Thus, the harmonic distortion on the ac side is still reasonable even under fault conditions. It is inevitable that the semiconductor devices now have to switch at a higher frequency than the equivalent switching frequency of SHE–PWM and, therefore, the switching losses of the power devices could increase.

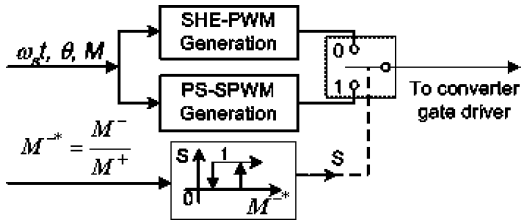
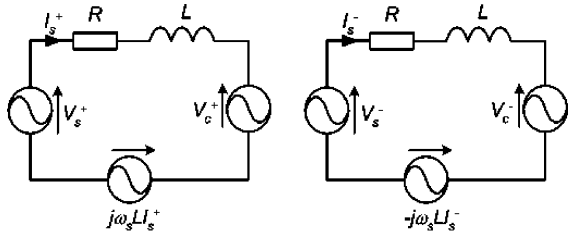


Fig. 9. Implementation of the proposed hybrid PWM strategy.



(a) (b)

Fig. 10. Simplified circuits of one end of the VSC transmission system in the positive sequence $(dq)^+$ frame rotating at a speed of $+\omega_s$ and negative sequence $(dq)^-$ frame rotating at a speed of $-\omega_s$. (a) $(dq)^+$ frame. (b) $(dq)^-$ frame.

It is anticipated that proper design should eliminate any problems associated with this higher switching frequency as the duration of a typical fault is fairly short. In addition, the current limit during such conditions can be reduced accordingly if required to lower the power losses.

Fig. 9 shows a schematic diagram of the proposed hybrid PWM where M^+ and M^- represent the positive and negative amplitudes of the controller outputs. During normal operation, as the unbalance is very small, the output S from the hysteresis controller is 0. Thus, the pulses generated by the SHE–PWM generator will be passed to the gate drivers to control the converter. If the unbalance increases, which causes M^- to increase, S becomes 1 and the outputs from the PS–SPWM generator are selected.

IV. VSC Transmission Analysis and Control

To analyze a VSC transmission under unbalanced voltage supply, the three-phase voltages and currents are usually decomposed into positive- and negative-sequence components. Due to the delta- or open-star connected transformer, zero-sequence components do not exist on the converter side. The simplified ac equivalent circuits for a VSC transmission system are shown in Fig. 10(a) and (b) in the positive $(dq)^+$ and negative $(dq)^-$ reference frames, respectively, where V_s and V_c are the source and converter output voltages, and ω_s is the angular frequency of the source voltage.

According to Fig. 10, in the $(dq)^+$ and $(dq)^-$ reference frames, the ac system can be expressed as [22]

$$\frac{d}{dt}\begin{bmatrix} i_{sd+}^{+} \\ i_{sq+}^{+} \end{bmatrix} = [A^+]\begin{bmatrix} i_{sd+}^{+} \\ i_{sq+}^{+} \end{bmatrix} + \frac{1}{L}\begin{bmatrix} v_{sd+}^{+} \\ v_{sq+}^{+} \end{bmatrix} - \frac{1}{L}\begin{bmatrix} V_{cd+}^{+} \\ V_{cq+}^{+} \end{bmatrix}$$
$$\frac{d}{dt}\begin{bmatrix} i_{sd-}^{-} \\ i_{sq-}^{-} \end{bmatrix} = [A^-]\begin{bmatrix} i_{sd-}^{-} \\ i_{sq-}^{-} \end{bmatrix} + \frac{1}{L}\begin{bmatrix} v_{sd-}^{-} \\ v_{sq-}^{-} \end{bmatrix} - \frac{1}{L}\begin{bmatrix} V_{cd-}^{-} \\ V_{cq-}^{-} \end{bmatrix} \quad (8a)$$

where

$$[A^+] = \begin{bmatrix} -\frac{R}{L} & \omega_s \\ -\omega_s & -\frac{R}{L} \end{bmatrix} \quad [A^-] = \begin{bmatrix} -\frac{R}{L} & -\omega_s \\ \omega_s & -\frac{R}{L} \end{bmatrix}. \quad (8b)$$

Superscripts $+$ and $-$ refer to the positive $(dq)^+$ and negative $(dq)^-$ reference frames while subscripts $+$ and $-$ refer to the positive and negative components.

The active and reactive power inputs at the transformer primary side are expressed as [22] and [25]

$$\begin{aligned} P_{\rm ac} &= P + P_{\sin 2}\cdot\sin(2\omega_s t) + P_{\cos 2}\cdot\cos(2\omega_s t) \\ Q_{\rm ac} &= Q \end{aligned} \tag{9a}$$

where P, $P_{\sin 2}$, $P_{\cos 2}$, and Q are given by

$$\begin{bmatrix} P \\ Q \\ P_{\sin 2} \\ P_{\cos 2} \end{bmatrix} = \frac{3}{2}\begin{bmatrix} V_{sd+}^{+} & V_{sq+}^{+} & V_{sd-}^{-} & V_{sq-}^{-} \\ -V_{sq+}^{+} & V_{sd+}^{+} & V_{sq-}^{-} & V_{sd-}^{-} \\ V_{sq-}^{-} & -V_{sd-}^{-} & -V_{sq+}^{+} & V_{sd+}^{+} \\ V_{sd-}^{-} & V_{sq-}^{-} & V_{sd+}^{+} & V_{sq+}^{+} \end{bmatrix}\begin{bmatrix} I_{sd+}^{+} \\ I_{sq+}^{+} \\ I_{sd-}^{-} \\ I_{sq-}^{-} \end{bmatrix}. \tag{9b}$$

Neglecting the converter power loss and considering the ac and dc power balancing equation, the dc-side system can be expressed as

$$C\frac{dV_{\rm dc}}{dt}\cdot V_{\rm dc} + I_{\rm dc}\cdot V_{\rm dc} = P_{\rm ac} \tag{10}$$

where $P_{\rm ac}$ is given by (9a) and (9b).

Under normal operation, one converter controls the dc voltage, namely the dc voltage controller (DCVC), and the other controls the transmitted active power, namely the active power controller (APC). Both converters can also perform independent reactive power (ac voltage) control. The positive and negative current references $i_{sdq+}^{+^*}$ and $i_{sdq-}^{-^*}$ are generated according to various control objectives (i.e., the requirements of $P_{\rm ac}$ and $Q_{\rm ac}$). During an asymmetrical fault, it may be preferred to eliminate the second harmonic power input to (or output from) the converter. Thus, there will be no second-order harmonic on the dc side and the operation of the healthy side network will not be affected. Therefore, referring to (9b), the two power oscillation terms $P_{\sin 2}$ and $P_{\cos 2}$ need to be zero. The $i_{sdq+}^{+^*}$ and $i_{sdq-}^{-^*}$ can then be calculated according to the values of P, Q, $P_{\sin 2}$, and $P_{\cos 2}$. For the DCVC, P usually comes from the dc voltage regulator while for the APC, P is set by the system operator.

The current loop is normally separated into two controllers (i.e., a positive-sequence current controller in the $(dq)^+$ frame and a negative-sequence current controller in the $(dq)^-$ frame [24]). The main challenge associated with such a design is to remove the interaction between the positive- and negative-sequence current controllers. This requires the decomposition of the positive- and negative-sequence components from the voltage and current. However, as the process of extracting the positive- and negative-sequence components (both current and voltage) involves considerable time delay, the system cannot be decoupled under transient conditions. To solve this problem, a new control method was proposed in [22] which uses a main controller and an auxiliary controller.

The current and voltage which contain both positive- and negative-sequence components can be expressed in the $(dq)^+$ frame as

$$\begin{aligned} I_{sdq}^{+} &= I_{sdq+}^{+} + I_{sdq-}^{+} = I_{sdq+}^{+} + I_{sdq-}^{-}\cdot e^{-j2\omega_s t} \\ V_{sdq}^{+} &= V_{sdq+}^{+} + V_{sdq-}^{+} = V_{sdq+}^{+} + V_{sdq-}^{-}\cdot e^{-j2\omega_s t}. \end{aligned} \tag{11}$$

Therefore, in the $(dq)^+$ frame, the system represented by (8) is expressed as

$$\begin{aligned} \frac{d}{dt}\left[I_{sdq+}^{+} + I_{sdq-}^{+}\right] &= \left[A^{+}\right]\left[I_{sdq+}^{+} + I_{sdq-}^{+}\right] \\ &\quad + \frac{1}{L}\left[V_{sdq+}^{+} + V_{sdq-}^{+}\right] - \frac{1}{L}\left[V_{cdq1}^{+} + V_{cdq2}^{+}\right] \end{aligned} \tag{12}$$

where V_{cdq1}^{+} and V_{cdq2}^{+} refer to the converter outputs controlled by the main and the auxiliary controllers, respectively.

The main controller uses decoupling control without involving any positive- and negative-sequence decomposition. Thus, V_{cdq1}^{+} is controlled as

$$V_{cdq1}^{+} = L\cdot\left[-U_{dq}^{+} + \left[A^{+}\right]\cdot\left(I_{sdq+}^{+} + I_{sdq-}^{+}\right)\right] + \left(V_{sdq+}^{+} + V_{sdq-}^{+}\right) \tag{13}$$

where U_{dq}^{+} is given by

$$U_{dq}^{+} = k_{p1}\left(I_{sdq+}^{+^*} - I_{sdq}^{+}\right) + k_{i1}\int\left(I_{sdq}^{+^*} - I_{sdq}^{+}\right)dt. \tag{14}$$

Substituting (13) and (14) into (12) and splitting into positive and negative subsystems, the dynamics of positive-sequence currents are then given by

$$\begin{aligned} I_{sd+}^{+}(s) &= \frac{\left(2\xi_{+}\omega_{n_+}s + \omega_{n+}^{2}\right)}{\left(s^2 + 2\xi_{+}\omega_{n_+}s + \omega_{n+}^{2}\right)}I_{sd+}^{+^*} \\ I_{sq+}^{+}(s) &= \frac{\left(2\xi_{+}\omega_{n+}s + \omega_{n+}^{2}\right)}{\left(s^2 + 2\xi_{+}\omega_{n+}s + \omega_{n+}^{2}\right)}I_{sq+}^{+^*} \end{aligned} \tag{15a}$$

where

$$\begin{aligned} \omega_{n+} &= \sqrt{k_{i1}} \\ \xi_{+} &= \frac{k_{p1}}{\left(2\sqrt{k_{i1}}\right)}. \end{aligned} \tag{15b}$$

Neglecting the integral term in (14), the dynamics of the negative-sequence current in the $(dq)^-$ frame are given by

$$\frac{d}{dt}\left[I_{sdq-}^{-}\right] = \begin{bmatrix} -k_{p1} & -2\omega_s \\ 2\omega_s & -k_{p1} \end{bmatrix}\left[I_{sdq-}^{-}\right] - \frac{1}{L}\left[V_{cdq2}^{-}\right]. \tag{16}$$

Based on (16), the auxiliary controller can be designed in the $(dq)^-$ reference frame by extracting the negative-sequence current. Similar ways as shown in (13) and (14) (i.e., containing a decoupling component and a PI regulator can then be used).

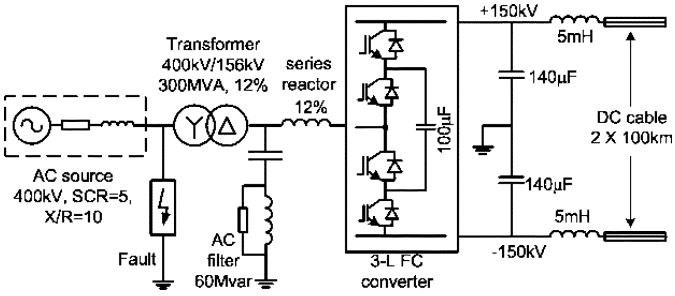


Fig. 11. Schematic diagram of one end of the simulated system.

However, due to the time delay involved into the decomposition of the positive- and negative-sequence currents, the system cannot achieve satisfactory decoupling under transient conditions. Instead, the so-called cross coupling control [22] is used and V_{cdq2}^{-} is given by

$$V_{cdq2}^{-} = L \cdot \begin{bmatrix} -k_d & -k_c \\ k_c & -k_d \end{bmatrix} \cdot \left[I_{sdq-}^{-*} - I_{sdq-}^{-} \right]. \quad (17)$$

Substituting (17) into (16) results in the dynamics of the negative-sequence currents becoming

$$I_{sd-}^{-}(s) = \frac{(k_d s + A_1) I_{sd-}^{-*} + (k_c s + A_2) I_{sq-}^{-*}}{\left(s^2 + 2\xi_- \omega_{n-} s + \omega_{n-}^2\right)}$$
$$I_{sq-}^{-}(s) = \frac{(-k_c s + A_2) I_{sd-}^{-*} + (k_d s + A_1) I_{sq-}^{-*}}{\left(s^2 + 2\xi_- \omega_{n-} s + \omega_{n-}^2\right)} \quad (18a)$$

where

$$A_1 = k_c (2\omega_s + k_c) + k_d (k_d + k_{p1})$$
$$A_2 = k_{p1} k_c - 2\omega_s k_d$$
$$\omega_{n-} = \sqrt{(k_d + k_{p1})^2 + (2\omega_s + k_c)^2}$$
$$\xi_- = \frac{k_d + k_{p1}}{\sqrt{(k_d + k_{p1})^2 + (2\omega_s + k_c)^2}}. \quad (18b)$$

The appropriate selection of k_{p1} and k_{i1} of the main controller can provide good control of the positive-sequence currents as indicated in (15). For the auxiliary controller, as the control parameters are chosen such that $A_1 \gg A_2$ is always met, according to (18), I_{sd-}^{-} and I_{sq-}^{-} follow their respective references and the interactions between the negative-sequence d- and q-axis currents are small.

V. System Studies

A VSC transmission system rated at 300 MW/$\pm$150 kV employing three-level FC converters was simulated using MATLAB/SIMULINK [26]. Fig. 11 shows one terminal of the simulated system. The previously described SHE–PWM control with nine switching angles per quarter cycle and the hybrid PWM were implemented. The frequency ratio of 15 was used for the implementation of the PS–SPWM. The FC voltage balancing control with PS–SPWM is based on the method proposed in [24] which adds small square correcting waveforms to the normal modulation signals. The objective for active power control during an asymmetrical fault is that the converter active power import/export does not contain any second-order power oscillations so that the other end of the ac network will not be affected by the fault while the system continues transmitting active power at a reduced level.

It is assumed that the main dc capacitor and FCs were initially charged at 300 kV and 150 kV, respectively, prior to enabling both converter stations. Both converters were enabled at 0.05 s and then various reactive and active power orders were applied to the APC. Reactive and active power orders of -100 MVar at a rate of 100 MVar/20 ms and -200 MW (inverter operation) at a rate of 100 MW/20 ms were applied at 0.1 s and 0.2 s, respectively. A single-phase-to-ground fault was applied to the APC side at 0.8 s and cleared at 1.0 s. The proposed FC voltage balancing control was initially enabled but was disabled at 0.57 s and re-enabled at 0.69 s. The maximum peak converter current was set at 2 kA. Selected simulation results for the APC side are shown in Fig. 12 when the APC operated as an inverter. It has been found that the waveforms for the DCVC are very similar to those shown in Fig. 12 but not shown in the paper due to space limitations.

Fig. 12(a)–(d) shows the positive- and negative-sequence current references and responses on the APC side. When a single-phase fault occurred at 0.8 s, the system switched from SHE–PWM to PS–SPWM control at around 0.82 s. It can be seen that the system performs well during active and reactive power variations. Both the positive- and negative-sequence currents are well controlled under single-phase fault conditions. Once the fault is cleared and after the system has gone back to normal operation, the system is switched back to SHE–PWM at 1.2 s. It has been found that the instant for switching back to SHE–PWM from PS–PWM should not solely rely on the measurement of M^{-} as small oscillations may exist but also need to include the negative-sequence current and voltage. Fig. 12(e) shows the main dc and FC voltages which indicate that both voltages are well controlled throughout the whole operating range. The power output from the converter depicted in Fig. 12(f) clearly shows that there is no second-order oscillation even during the single-phase-to-ground fault. The voltage THD shown in Fig. 12(g) is around 2% during steady-state.

The effectiveness of the FC voltage control with SHE–PWM is further illustrated in Fig. 13(a) and (b). When the FC voltage balancing control is disabled at 0.57 s, the FC voltage moves away from the desired value of 150 kV but quickly moves back after it is re-enabled at 0.69 s. The ac voltage THD is increased during the period of 0.57 s–0.69 s due to the increase of the FC voltage unbalance.

The phase voltage and current waveforms around the time of the switching from SHE–PWM to PS–SPWM at 0.82 s are shown in Fig. 14(a) and (b), respectively. As can be seen, the switching between the two PWM methods was very smooth. Similar results were obtained when the system is switched back from PS–SPWM to SHE–PWM but are not shown here once again due to space limitations.

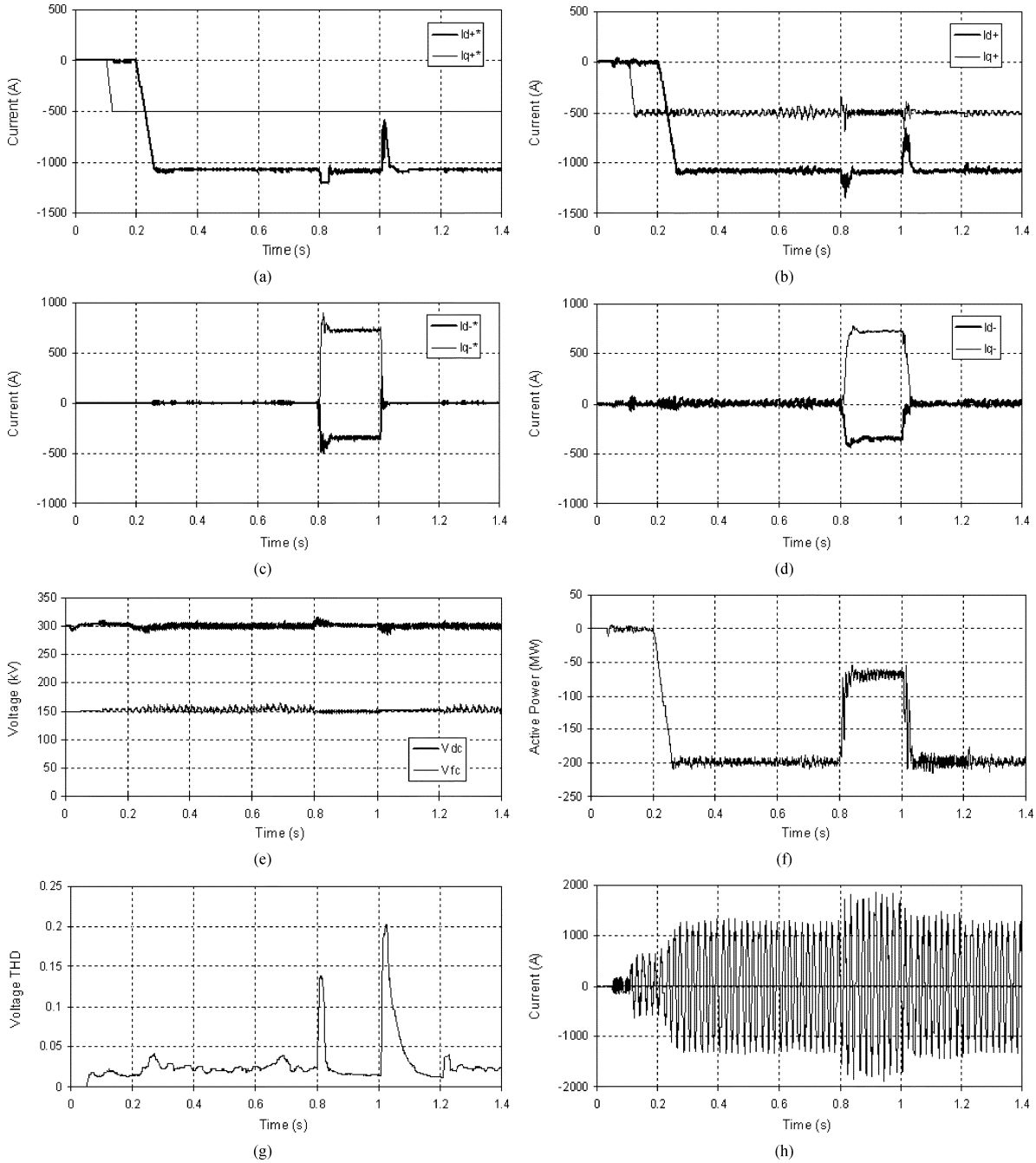


Fig. 12. Simulated waveforms on the APC side (FC voltage control disabled at 0.57 s and re-enabled at 0.7 s, single-phase-to-ground fault applied at 0.8 s and cleared at 1.0 s, converter switched back to SHE–PWM control at 1.2 s). (a) Converter positive d–q current references. (b) Converter positive d–q current responses. (c) Converter negative d–q current references. (d) Converter negative d–q current responses. (e) Main dc and flying capacitor voltages. (f) Active power input measured at the converter side. (g) AC voltage THD. (h) Converter ac phase current.

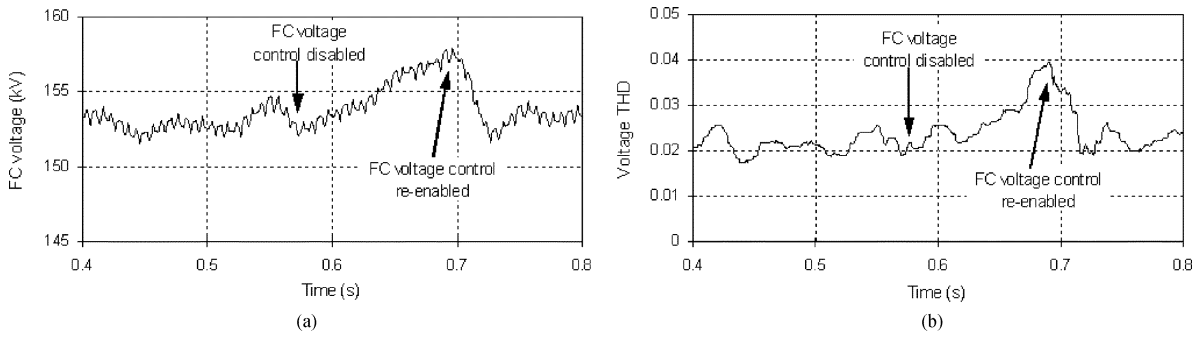


Fig. 13. Effect of FC voltage control with SHE–PWM. (a) Filtered FC voltage. (b) AC voltage THD.

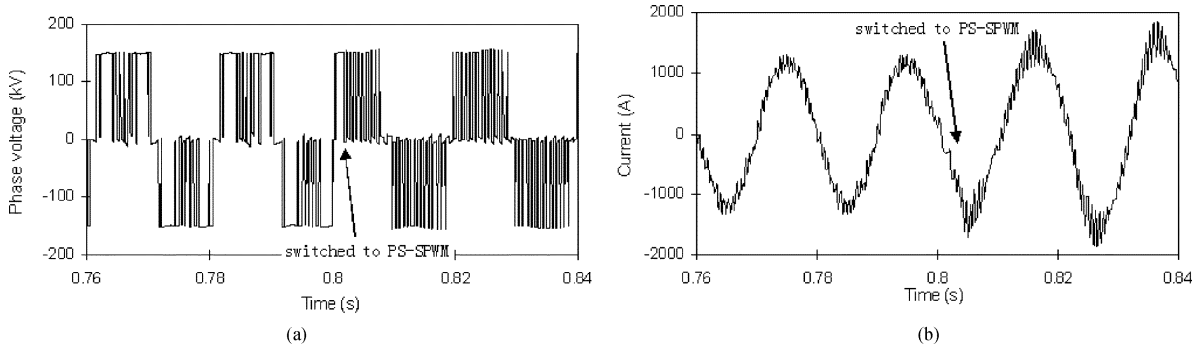


Fig. 14. Snapshots of voltage and current waveforms around the time of asymmetric fault (fault occurred at 0.8 s, SHE–PWM switched to PS–SPWM at 0.82 s). (a) Phase voltage. (b) Phase current.

VI. Conclusion

A VSC transmission system based on three-level FC converters and hybrid PWM control is studied in this paper. SHE–PWM is used during balanced network conditions and is switched to PS–SPWM during an asymmetrical network fault. The generation of the switching patterns under SHE–PWM for each power device is described taking into account the natural balancing of the FC voltage. FC voltage balancing control has been investigated and a method based on the slight modification of the firing angles to change the charging and discharging period of the FC has been proposed. The FC voltage ripple under SHE–PWM is estimated and compared to that under PS–PWM control. The circuits for implementation of SHE–PWM for the three-level FC converter are illustrated. Simulation studies on a 300 MW/±150-kV system show the effectiveness of the hybrid PWM and the FC voltage balancing strategy. This type of VSC transmission system has low switching power loss and provides satisfactory response even under severe single-phase fault operating conditions.

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Lie Xu (M'03–SM'06) received the B.Sc. degree in electrical and electronic engineering from Zhejiang University, Hangzhou, China, in 1993, and the Ph.D. degree in electrical and electronic engineering from the University of Sheffield, Sheffield, U.K., in 1999.

Currently, he is with the School of Electronic, Electrical Engineering, and Computer Science, Queen's University of Belfast, Belfast, U.K. Previously, he was with ALSTOM T&D, Stafford, U.K., from 2001–2003 and with the Centre for Economic Renewable Power Delivery (CERPD), University of Glasgow, Glasgow, U.K., from 1999 to 2000. His main interests are power electronics, renewable energy, and application of power electronics to power systems.

Vassilios G. Agelidis (SM'00) was born in Serres, Greece. He received the B.S. degree in electrical engineering from Democritus University of Thrace, Thrace, Greece, in 1988, the M.S. degree in applied science from Concordia University, Montreal, QC, Canada, in 1992, and the Ph.D. degree in electrical engineering from the Curtin University of Technology, Perth, Australia, in 1997.

From 1993 to 1999, he was with the School of Electrical and Computer Engineering, Curtin University of Technology. In 2000, he joined the University of Glasgow, Glasgow, U.K., as a Research Manager for the Centre for Economic Renewable Power Delivery. In addition, he has authored/coauthored several journal and conference papers as well as the book *Power Electronic Control in Electrical Systems* (Elsevier, 2002). In 2005, he was appointed the inaugural Chair of Power Engineering in the School of Electrical, Energy and Process Engineering, Murdoch University, Perth, Western Australia.

Dr. Agelidis received the prestigious Advanced Research Fellowship from the Engineering and Physical Sciences Research Council (EPSRC) in 2004. He is the Vice President of Operations within the IEEE Power Electronics Society. He was an Associate Editor of the IEEE POWER ELECTRONICS LETTERS from 2003 to 2005, and served as the Power Electronics Society Chapter Development Committee Chair from 2003 to 2005. He will be the Technical Chair of the 39th IEEE PESC'08 in Rhodes, Greece.