Self-cleaning Photovoltaic (PV) Modules

Student:
Nur Ain Noor Hisham

Supervisor:
Dr David Parlevliet

Submission Date:
1/12/2017
Acknowledgement

My deepest gratitude to my supervisor, Dr David Parlevliet for his generous guidance, support and help throughout completing this thesis project. I would also like to thank you everyone else involved as my thesis project could not be completed without the help and guidance from:

- Dr. Gareth Lee, senior lecturer for his guidance and advice in troubleshooting microcontroller programming.
- Mr Mark Burt, technical officer for his tremendous advice and physical mounting construction and providing me with the necessary supplies and equipment.
- Mr Graham Malzer, technical officer for his technical help and advice.
- Mr Iafeta Laava, technical officer for his help and advisory for circuit construction, wiring and electrical component supplies such as the PROVA.
- Nazirul Haziq Kamarudin, 4th Year ICS student for support and advice troubleshooting microcontroller programming.

Lastly, I would like to thank my family and friends for the continuous support in completion of this project.
Disclaimer

I hereby declare that this thesis project is of my own work unless stated otherwise with proper acknowledgement of the cited reference.
Abstract

The effect of soiling accumulation towards photovoltaic (PV) could cause a reduction in the PV system performance. The decrease in PV system output due to soiling has been proven crucial (Jiang, Lu, and Sun 2011). Thus signifies the significance of further research on the effect of soiling on a PV system. This project is a research based on the climate in Murdoch, Western Australia. This project consists of three parts; Photovoltaic (PV) performance testing, Air quality testing, Light transmittance testing. The PV performances were analysed based on three different dust mitigation conditions. The first module labelled as A is washed regularly as part of the dust mitigation strategies applied. The second module, labelled as B has a hydrophobic coating which functions when rainwater fall on the panel, the water would roll off the module at the same time rolling dust off the module. The third module, labelled as C is kept without any dust mitigation method. All three modules were tested out and washing performs the best giving a reduction in performance of 30.8% after 18 days, while B reduces in 47.4% performance and C has a 31.4% reduction in performance. Test 2 involves correlating the air quality with the dust accumulation on the PV modules. An optical dust sensor is used for this test. Test 3 has the same concept as Test 2 but is more closely related to the dust adhering to the PV modules. A glass panel is used to simulate the dust accumulation with a Light Emitting Diode (LED) and an Light Dependent Resistor (LDR) in between. A ratio-based calculation is made for test 3 to correlate the transmittance with voltage output and comparing the value when the glass is clean compared to dirty. The washed module performs the best with an average air quality of 0.025mg/m³. The worst module was the one without dust mitigation strategies, where the light transmittance reduced in 22% after two weeks of dust accumulation.

Consequently, to improve the performance of the PV in the industry, soiling should not be ignored as it should be a big issue in the PV industry.
List of Figures

Figure 1: Water drop taking up the dust particles (Nanoman 2017) ......................... 13
Figure 2: Light Transmission Testing (Sipitakiat 2003) ........................................... 14
Figure 3: Amorphous silicon cell structure (Maehlum 2015) ............................... 16
Figure 4: Efficiency comparisons of thin-film technologies (Energy and Systems 2017) ... 17
Figure 5: Fill factor of PV (PVcdrom 2017) .......................................................... 17
Figure 6: Global annual production of PV in the world (Energy and Systems 2017) .... 18
Figure 7: Percentage of global annual PV production in 2016 (Energy and Systems 2017) ......................................................................................................................... 19
Figure 8: Market share of Thin-Film technologies (Energy and Systems 2017) ........... 19
Figure 9: PV module production of a-Si (Energy and Systems 2017) ....................... 20
Figure 10: Transmittance reduction due to dust deposition (Elminir et al. 2006) ....... 21
Figure 11: Example of Soiling Ratio values (Homer 2018) ....................................... 24
Figure 12: Dust accumulation at the bottom edge of the frames (Energy 2017) ........... 25
Figure 13: Design feature of the project ................................................................. 29
Figure 14: Dust measuring system ........................................................................ 32
Figure 15: PV panels interface with PROVA ........................................................... 34
Figure 16: Interface of the Optical Dust Sensor (Instructables 2017) ......................... 35
Figure 17: Wiring inside the enclosure ................................................................. 36
Figure 18: Autocad design for light transmittance testing ...................................... 37
Figure 19: Position of LED and LDR for light transmittance testing ....................... 37
Figure 20: Arduino interface with digital outputs and analog inputs ....................... 38
Figure 21: CL50 glass cleaner ................................................................................ 39
Figure 22: Hydrophobic coating NG-1314/D ............................................................ 40
Figure 23: ICSP headers on the Arduino (Arduino 2017) ...................................... 41
Figure 24: SPI communication protocol (Sfuptownmaker 2017) ............................ 42
Figure 25: I²C communication protocol (Sfuptownmaker 2017) ............................ 42
Figure 26: SDA and SCL connection on the Arduino Uno board ............................. 43
Figure 27: Transmitter and receiver pins for serial communications on the Arduino ............................... 43
Figure 28: Libraries used in the Arduino program .................................................. 45
Figure 29: Declaration of input and output types and pins ...................................... 45
Figure 30: Void setup program ............................................................................ 46
Figure 31: The start of the void loop program ....................................................... 47
Figure 32: LED and LDR loop program ................................................................ 47
Figure 33: Setting the time for the RTC ............................................................... 48
Figure 34: Program to display the analog input and digital output ....................... 48
Figure 35: Data variable created ........................................................................ 49
Figure 36: Creating a file to write to the SD card and time delay program ............... 49
Figure 37: Climate conditions in Perth during the summer ................................. 50
Figure 38: Comparison of IV curve before and after correction to STC ................... 51
Figure 39: Comparison of Power Curve before and after correction to STC .......... 52
Figure 40: Panel A before and after 2 weeks of dust mitigation ............................. 53
Figure 41: Panel A performance ......................................................................... 54
Figure 42: Panel B before and after 2 weeks of dust mitigation ............................. 55
Figure 43: Panel B performance ......................................................................... 56
Figure 44: Panel C before and after 2 weeks of dust mitigation ............................. 57
Figure 45: Panel C performance ......................................................................... 58
Figure 46: PV panels performance ....................................................................... 59
Figure 47: Decrement in performance of PV modules ......................................... 60
Figure 48: The soiling accumulation of the PV modules after 2 weeks ................. 61
Figure 49: Change in power supply from DC to AC .......................................... 62
Figure 50: Enclosure mounting ......................................................................... 62
Figure 51: Soiling Ratio Calculation ................................................................... 67
Figure 52: Sample data logging file from Arduino SD card ................................... 68
List of Tables

Table 1: Dust mitigation strategies applied to each PV panel ........................................... 12
Table 2: Summary of thin-film technology (Maehlum 2015) ............................................ 15
Table 3: Specification for Arduino UNO Rev3 SMD (Lahfaoui et al. 2017) ...................... 30
Table 4: Amorphous PV panel specifications (Jaycar 2017) ............................................ 31
Table 5: PV performance analysis with the methodology applied .................................... 33
Table 6: Standard Test Conditions of PV ................................................................. 34
Table 7: Connection from Arduino board to the optical dust sensor ................................ 36
Table 8: SPI pins on Arduino Uno (Arduino 2017) .................................................... 41
Table 9: Variable declarations .............................................................................. 44
Table 10: Parameters used for correction to STC ...................................................... 51

List of Equations

Equation 1: Reduction in Transmittance ...................................................................... 22
Equation 2: Soiling Ratio based on short circuit current ............................................. 23
Equation 3: Soiling Ratio based on open circuit voltage .............................................. 23
Equation 4: New corrected current at STC ................................................................. 28
Equation 5: New corrected voltage at STC ................................................................. 28
Equation 6: Voltage calculation based on raw value from Arduino ............................ 47
List of Abbreviations

AC  Alternating Current
A-si  Amorphous Silicon
ASTM  American Society of Testing Material
C  Calibration constant during initial calibration
CdS  Cadmium Sulphide
CdTe  Cadmium Telluride
CIGS  Copper Indium Gallium Selenide
DC  Direct Current
DCS  Distributed Control System
eV  Electron-volt
FF  Fill Factor
G  Irradiance
I  Current
I\textsuperscript{P}C  Inter-integrated Circuit
ICSP  In-Circuit Serial Programming
IEC  International Electrotechnical Commission
I_{SC}  Short Circuit Current
LDR  Light Dependent Resistor
LED  Light Emitting Diode
MISO  Master In-Slave Out
MOSI  Master Out-Slave In
NOCT  Normal Operating Cell Temperature
PECVD  Plasma-Enhanced Chemical Vapour Deposition
P_{MAX}  Maximum Power
PV  Photovoltaics
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PWM</td>
<td>Pulse Width Modulation</td>
</tr>
<tr>
<td>ROW</td>
<td>Rest of the World</td>
</tr>
<tr>
<td>Rs</td>
<td>Internal series resistance</td>
</tr>
<tr>
<td>Rx</td>
<td>Receiver</td>
</tr>
<tr>
<td>SCK</td>
<td>Serial Clock</td>
</tr>
<tr>
<td>SCL</td>
<td>Clock Signal</td>
</tr>
<tr>
<td>SDA</td>
<td>Data Signal</td>
</tr>
<tr>
<td>SPI</td>
<td>Serial Peripheral Interface</td>
</tr>
<tr>
<td>SR</td>
<td>Soiling Ratio</td>
</tr>
<tr>
<td>SS</td>
<td>Slave Select</td>
</tr>
<tr>
<td>STC</td>
<td>Standard Test Conditions</td>
</tr>
<tr>
<td>TCO</td>
<td>Transparent Conductive Oxides</td>
</tr>
<tr>
<td>TpV</td>
<td>Temperature of module</td>
</tr>
<tr>
<td>Tref</td>
<td>Temperature of reference condition</td>
</tr>
<tr>
<td>Tx</td>
<td>Transmitter</td>
</tr>
<tr>
<td>V</td>
<td>Voltage</td>
</tr>
<tr>
<td>V_{oc}</td>
<td>Open Circuit Voltage</td>
</tr>
</tbody>
</table>

**List of Symbols**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \rho_D )</td>
<td>Density of Dust Deposited</td>
</tr>
<tr>
<td>( \Delta \tau )</td>
<td>Reduction in Transmittance</td>
</tr>
<tr>
<td>( k )</td>
<td>Curve correction factor</td>
</tr>
<tr>
<td>( \alpha )</td>
<td>Coefficient of temperature at short circuit current</td>
</tr>
<tr>
<td>( \beta )</td>
<td>Coefficient of temperature at open circuit voltage</td>
</tr>
<tr>
<td>( \gamma )</td>
<td>Coefficient of temperature at maximum power</td>
</tr>
<tr>
<td>( \Omega )</td>
<td>Ohms</td>
</tr>
</tbody>
</table>
# Table of Contents

Acknowledgement .................................................................................................................. 2

Disclaimer ................................................................................................................................. 3

Abstract .................................................................................................................................. 4

List of Figures ........................................................................................................................... 5

List of Equations ....................................................................................................................... 6

List of Abbreviations ............................................................................................................... 7

List of Symbols ......................................................................................................................... 8

1. Introduction ......................................................................................................................... 11
   1.1. Problem Statement ........................................................................................................ 11
   1.2. Project Objectives ......................................................................................................... 11

2. Project Background .............................................................................................................. 12
   2.1. The effect of Soiling on the Performance of the PV panels ........................................... 12
   2.2. Transmittance of Light and Dust Density Sensing ......................................................... 14

3. Literature Review ................................................................................................................ 15
   3.1. Amorphous Silicon Cells ............................................................................................... 15
       3.1.1. Overview ................................................................................................................. 15
       3.1.2. Structure ................................................................................................................. 16
       3.1.3. Performance .......................................................................................................... 16
       3.1.4. Market Share ......................................................................................................... 18
   3.2. Soiling on Photovoltaic Panels ....................................................................................... 21
       3.2.1. The Effect of Soiling on Photovoltaic Panels ........................................................... 21
       3.2.2. Measuring Soiling on PV systems ............................................................................ 23
       3.2.3. Effect of Soiling Non-Uniformity ............................................................................ 25
   3.3 Dust Mitigation Strategies ............................................................................................... 26
       3.3.1 Natural Dust Removal ............................................................................................... 26
       3.3.2 Mechanical Dust Removal ....................................................................................... 26
       3.3.3 Hydrophobic Coatings Dust Removal ..................................................................... 27
       3.3.4 Electrostatic Dust Removal ...................................................................................... 27
   3.4 Standard Test Conditions Correction Procedure ............................................................. 28

4. Design specifications and features ...................................................................................... 29
   4.1 Arduino ............................................................................................................................. 30

5. Project Methodology ............................................................................................................ 32
   5.1 Dust Measuring System ................................................................................................. 32
       5.1.1 PV Performance Testing ........................................................................................ 33
       5.1.2 Optical Air Quality Sensor ...................................................................................... 35
5.1.3. Transmittance of Light ................................................................. 37

5.2 Dust Mitigation System ................................................................. 39
  5.2.1 Scheduled washing of PV modules ......................................... 39
  5.2.2 Hydrophobic coatings ............................................................ 40

5.3 Arduino Programming ................................................................. 41
  5.3.1 Communication Protocols ..................................................... 41
  5.3.2 Variables ............................................................................. 44
  5.3.3 Detailed Program ................................................................. 45

6 Results and Discussions .............................................................. 50
  6.1 Climate during Experiment ....................................................... 50
  6.2 Correction procedure of the IV Curve of the PV .................... 51
  6.3 PV Performance .................................................................... 53
    6.3.1 Panel A .......................................................................... 53
    6.3.2 Panel B .......................................................................... 55
    6.3.3 Panel C .......................................................................... 57
    6.3.4 Overall ........................................................................... 59

7 Problems Encountered and Countermeasures ............................ 62
  7.1 Power Supply ......................................................................... 62
  7.2 Weatherproof Conditions on Electrical Wirings ..................... 62

8 Conclusion and Future Works ..................................................... 63
  8.1 Project Conclusion .................................................................. 63
  8.2 Future Work Recommendations ............................................. 64

9 References .................................................................................... 65

10 Appendices .................................................................................. 67
  10.1 Appendix A: Calculation for Soiling Ratio ............................ 67
  10.2 Appendix B: Data logging from Arduino Programming Sample ................................................................................. 68
1. Introduction

1.1. Problem Statement

Research and development of Photovoltaic (PV) systems has been mainly focused on the availability of radiance, sizing and optimization of operating the systems. However, the effect of dust and soiling accumulation towards the PV system has lacked attention (Elminir et al. 2006). Dust build-up on the PV modules could cause a reduction in PV systems output. The degradation in performance due to soiling on PV systems have been proven crucial; with dust mitigation of $22g/m^2$, the reduction in PV module efficiency can decrease up to 26% (Jiang, Lu and Sun 2011). This highlights the significance of self-cleaning the PV modules to ensure PV systems operate at a higher performance. Thus, signifies the need for self–cleaning PV systems especially in areas where rainfall statistically is low and sandstorms are common.

1.2. Project Objectives

The aim of this thesis is to measure the dust and soiling on the PV modules. This signifies the significance of PV systems with self–cleaning mechanism. Other objectives include:

- To design and build a Photovoltaic (PV) modules standalone system for soiling accumulation measurements.
- To perform a controlled testing of the system on the level 3 of the Engineering Building.
- To identify and implement dust mitigation strategies for the self-cleaning PV modules
- To investigate the performance of the PV modules with different types of dust mitigation strategies applied.
- To evaluate and interpret the IV curves to the Standard Test Conditions (STC).
2. Project Background

This thesis project is composed of two sections. The first part of the project is to design a standalone photovoltaic (PV) system that measures the effect of dust accumulation on the PV panels. The performance of the PV systems is monitored by using an optical dust sensor and analysing the reduction in the efficiency of the PV panels after being tested in the outdoor testing area.

The second part of the project involves applications of dust mitigation strategies on PV panels. Several dust mitigations strategies could be applied to make sure the efficiency of the PV system is kept high. Part of the project plan is to compare the effect of 3 types of PV panels under different conditions; the first panel has a layer of Nano-film coating, the second panel is scheduled for water spraying at certain time intervals and the last panel is left without any dust mitigation strategies.

2.1 The effect of Soiling on the Performance of the PV panels

For this thesis project, there will be two soiling mitigation method applied; a PV panel with scheduled washing using a timer and another PV panel with Nano-film coating. These two panels will be compared with a third PV panel that has no dust mitigation strategies applied. Table 1 below shows the application of each PV panels.

<table>
<thead>
<tr>
<th>PV Panel</th>
<th>DUST MITIGATION STRATEGIES APPLIED</th>
</tr>
</thead>
<tbody>
<tr>
<td>Panel A</td>
<td>Scheduled washing</td>
</tr>
<tr>
<td>Panel B</td>
<td>Nano-film hydrophobic coating</td>
</tr>
<tr>
<td>Panel C</td>
<td>Not applicable</td>
</tr>
</tbody>
</table>

*Table 1: Dust mitigation strategies applied to each PV panel*
The tilt angle to all three modules of the system is standardised to a fixed value. The PV system is set at tilt angle of 32°.

Panel A (Scheduled washing)

This panel will be constructed with a built-in washing system that is operated based on a timer. The principle of the operation of this panel is similar to a water sprinkler system. However, in constructing this system, programming is required to ensure scheduled washing of the panel. Arduino is used to program the scheduled washing of the PV panel. A weather box is necessary to make sure the wirings are protected from harsh weather conditions.

Panel B (Nano-film Coating)

Panel B is sprayed with a nano-film hydrophobic coating which repels water from the panel. The coating helps the rainwater to roll off the PV panel with the dirt and dust (Nanoman 2017). Thus, reducing the frequency of cleaning required which acts as initial investment to the PV system in cost and energy saving. This can be shown in Figure 1 below.

Panel C

Panel C is left without any dust mitigation strategies. This is to compare the effect of dust accumulation on a panel with and without dust mitigation strategies applied.
2.2. Transmittance of Light and Dust Density Sensing

A light transmittance test through a glass sheet and an air quality testing is conducted to analyse the PV panel performance. The transmittance of light is tested out using a glass sheet in the middle of a light emitting diode (LED) and a light dependent resistor (LDR) as detectors. The glass is where dust accumulates, resisting light transmission from the LED to the LDR. The decrease in light intensity due to the dust build-up then increases the resistance of the LDR, hence lowering the current and voltage (Electronics Tutorial 2017). This is from Ohm’s Law where resistance is inversely proportional to current. Figure 2 below shows the alignment of the LED, LDR and the glass for light transmittance testing.

For an accurate representation of the result, the test is conducted during night time where there will be no external sunlight variations affecting the results. The air quality, on the other hand, is tested out using a compact optical dust sensor as per used in-house air purifiers. The optical dust sensor used is of brand Sharp with model number of GP2Y1010AU0F (Sharp 2017).
3. Literature Review

3.1. Amorphous Silicon Cells

3.1.1. Overview

Amorphous silicon solar cells are categorized in the silicon thin-film category which involves several layers of photovoltaic material deposition on a substrate (Maehlum 2013). The shape of the cell is not structured which suits the name of the cell, amorphous, meaning without a clearly defined form.

The development of amorphous silicon (a-Si) based solar cell has significantly improved in performance and production, with more than 200 peak megawatts (MWp) annually from 2009 until 2011 (Fraunhofer Institute for Solar Energy Systems 2017). Amorphous silicon thin films were deposited by plasma-enhanced chemical vapour deposition (PECVD). One of the niche applications of the cells is to power electronics calculators (Shah 2012). Table 2 below shows an overview of how a-Si cells compare to other thin-film technology.

<table>
<thead>
<tr>
<th></th>
<th>Amorphous Silicon (a-Si)</th>
<th>Cadmium Teluride (CdTe)</th>
<th>Copper Indium Gallium Selenide (CIGS)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Efficiency</strong></td>
<td>8.1%</td>
<td>14.4%</td>
<td>14.5%</td>
</tr>
<tr>
<td><strong>Market share in thin film technology</strong></td>
<td>32%</td>
<td>43%</td>
<td>25%</td>
</tr>
<tr>
<td><strong>Advantages</strong></td>
<td>Old technology Excellent for small devices</td>
<td>Low manufacturing cost</td>
<td>High efficiency Glass or flexible substrates</td>
</tr>
<tr>
<td><strong>Disadvantages</strong></td>
<td>Low efficiency High cost equipment</td>
<td>Medium efficiency Requires use of Cadmium which is is highly toxic</td>
<td>Medium efficiency High cost Requires less cadmium than CdTe solar cells.</td>
</tr>
<tr>
<td><strong>Major manufacturers</strong></td>
<td>Sharp</td>
<td>First Solar</td>
<td>Solar Frontier</td>
</tr>
</tbody>
</table>

*Table 2: Summary of thin-film technology (Maehlum 2015).*
3.1.2. Structure

The operation and efficiency of the a-Si cells depends on the different properties of the material, as to compare with crystalline silicon cells. A-si has a different fundamental cell structure which the cells is heterojunction into p-i-n and n-i-p structures rather than the standard n/p junction of a basic silicon cell(Carlson and Wronski 2003). The structural arrangement of the layering for an a-Si cell is seen in Figure 3 below.

![Amorphous silicon cell structure](image)

*Figure 3: Amorphous silicon cell structure(Maehlum 2015).*

3.1.3. Performance

Amorphous silicon cells have a significantly higher temperature resistance than the basic crystalline cells. In addition to that, the cells is also flexible which serves as a benefit in increasing potential application of the cell (Maehlum 2015). However, there are several downsides to using an amorphous silicon cell. One of the cons is having lower efficiency hence, requiring a larger scale system of a-Si based cells to produce the same amount of power a typical crystalline PV system produces. Other than that, thin films cells have a faster initial degradation rate compared to crystalline silicon-based cells. (Maehlum 2015)
Nowadays, the average efficiency of an a-Si cell is ranged at 6-8%, in which it has a lower performance rate compared to a crystalline silicon cell. Nevertheless, Fraunhofer reported 14% high efficiency of an a-Si based cell by applying a triple-junction cell (Fraunhofer Institute for Solar Energy Systems 2017). This can be seen from Figure 4 below.

Moreover, with a triple-junction cell, the light-induced degradation is 10-15% which is lower than a single-junction cell, having 18-30%. However, the light-induced degradation also depends on the thickness of the i-layer of the cell structure (Carlson and Wronski 2003).

The fill factor (FF) is also a measurement for analysing the PV performance. FF is a theoretical representation of the power generation of the solar cell. Figure 5 above shows how FF is measured. FF measures the ratio of maximum power to the $V_{oc}$ and $I_{sc}$. For an ideal solar cell, the FF value is 1, indicating no energy losses. Practically a solar cell will have an FF value of lower that 1. This highlights that the closer the value of FF to 1, the better the performance of the solar cell.

![Figure 4: Efficiency comparisons of thin-film technologies (Fraunhofer Institute for Solar Energy Systems 2017).](image)

![Figure 5: Fill factor of PV (PVcdrom 2017).](image)
3.1.4. Market Share

Photovoltaic technology has been expanding worldwide over the past years and plays a significant role in sustainable energy towards unlimited access to energy. Taking China as an example, China has a 232 MWp high demand for new solar modules every year since 2012. China’s government has also announced an interest in expanding the capacity of PV installation up to 1800 MWp by 2020 (Jiang, Lu, and Sun 2011).

The industry has taken a positive turn due to growth in technology and economy worldwide. This is highlighted in Figure 6 and Figure 7 below, where the trend of the graph inclines as the years go by. The global annual production shows that China and Taiwan hold the lead with a 55GWp annual global output which is 26% of the world in 2016, followed by the rest of the world (ROW) with 15GWp, North America, Europe and Japan (Jiang, Lu, and Sun 2011).

![Figure 6: Global annual production of PV in the world (Fraunhofer Institute for Solar Energy Systems 2017).](image-url)
Regarding market share based on photovoltaic technology, the highest share is accounted by silicon cells with approximately 94% of the total production of PV in 2016. Thin film cells however, has a market share about 6% of the total yearly production.

Nonetheless, this does not signify the declination of demand and production of thin-film cells. The a-Si technology production is growing in 2009 to 2011. The highest percentage of market share held by CdTe is in 2009 where it is accounted for 76.47% of the market share as seen in Figure 8 below.
Figure 9 below shows that a-Si based PV technology is the second highest in demand thin-film PV technology in the market until 2012. However, there is a declination in a-Si production after 2012. CdTe leads the market with a 3.1GWp production, followed by Copper Indium Gallium Selenide (CIGS) with a 1.3GWp, then Amorphous Silicon (a-si) with 0.5GWp.

![Figure 9: PV module production of a-Si(Fraunhofer Institute for Solar Energy Systems 2017)](image)
3.2 Soiling on Photovoltaic Panels

3.2.1. The Effect of Soiling on Photovoltaic Panels

Two major concerns are compromising the performance of a photovoltaic module. These include soiling and overheating (Saidan et al. 2016). Soiling is a term referring to dust accumulation, bird droppings and plant growth contaminations.

The effect of soiling to a photovoltaic (PV) module is closely related to the performance of the module. This is due to the restriction in light transmittance due to soil build-up which is reflected by Figure 10. The experiment from Figure 10 below was conducted in the western Egyptian desert with the low amount of rainfall (Elminir et al. 2006). This highlights the degradation of the output of the PV panels when being unattended.

![Figure 10: Transmittance reduction due to dust deposition. (Elminir et al. 2006)](image-url)
Equation 1 has been empirically fitted based on the pattern of the 2 variables from Figure 10 above. (Elminir et al. 2006)

\[
\Delta \tau = 0.0381 \rho_D^4 - 0.8626 \rho_D^3 + 6.4143 \rho_D^2 - 15.051 \rho_D + 16.769
\]

*Equation 1: Reduction in Transmittance*

Given that:

\[
\Delta \tau : \text{Reduction in transmittance} \ [\%]
\]

\[
\rho_D : \text{Density of dust deposited} \ [g/m}^3]
\]

The transmittance of light could be incremented by decreasing the angle of the PV panels. A PV panel perpendicularly facing the sun produces more energy compared to PV panels that is slightly inclined. However, this would directly cause higher dust deposition since dust mitigation by gravity does not apply to PV panels in perpendicular configurations. The average reduction in light transmission of a PV module at a horizontal plane is 27.62% (Elminir et al. 2006). Despite the angle of the PV module being at a tilt angle of 0°, there is still a reduction in light transmission through the PV modules. Thus, signifies the importance of keeping the PV modules clean and dust-free to avoid further reduction in light transmittance into the PV modules.

The effect of soiling is closely related to the tilt angle of the PV panel. A higher tilt angle would have lesser dust deposition. However, the angle affects solar irradiation exposed to the PV panel. An optimal angle for Perth would be 31.9°, facing North on a roof (Australian PV Association 2009).

From an analysis of an experiment conducted in Singapore, the author claims that dust accumulation decreases when the PV panels are placed facing the wind (Hee et al. 2012). Based on this information, PV panels could be constructed facing towards the wind direction.
to minimize dust deposition. However, this is only applicable if the wind direction does not affect the ability of the solar cells to gather light.

3.2.2. Measuring Soiling on PV systems

Soiling on PV modules is measured using the soiling ratio. This method is performed by comparing two soiling ratio (SR) metrics, short circuit current soiling ratio (SR$^{isc}$) and maximum power soiling ratio (SR$^{pmax}$). Soiling rate is perceived as the reduction in irradiation received by the PV modules due to soiling. Soiling ratio is the difference in dust measurement of a dirty module to a clean. SR$^{isc}$ is the soiling ratio at which the current in the module at the value of the short circuit current. SR$^{pmax}$ is the soiling ratio at which power of module is maximum (Gostein et al. 2013). This is calculated using the below Equation 2 and Equation 3, where subscript “1” refers to clean module and “2” refers to dirty modules (Homer 2018):

$$SR^{isc} = \frac{G_2}{G_1} = \frac{C_2^{isc}(1-\alpha(T_{PV2} - T_{REF})).ISC_2}{C_1^{isc}.(1-\alpha(T_{PV1} - T_{REF})).ISC_1}$$

**Equation 2: Soiling Ratio based on short circuit current**

$$SR^{pmax} = \frac{C_2^{pmax}(1-\gamma(T_{PV2} - T_{REF})).Pmax_2}{C_1^{pmax}.(1-\gamma(T_{PV1} - T_{REF})).Pmax_1}$$

**Equation 3: Soiling Ratio based on open circuit voltage**

Where:-

- $G$: Irradiance
- $C$: Calibration constant that relates the short circuit current or maximum power during initial calibration to the irradiance at the reference condition.
- $\alpha$: Coefficient of temperature at short circuit current
- $T_{PV}$: Temperature of module
- $T_{REF}$: Temperature of reference condition
- $\gamma$: Coefficient of temperature at maximum power
- $ISC$: Short circuit current
- $P_{MAX}$: Maximum power
The $\gamma$ of a-si cell is 0.268 (Chakraborty et al. 2017) with a $\alpha$ of 0.0001 (Blagojevic 2016). In real world application, the coefficient values could be quite diverse depending on the behaviour of the solar cell. The values of coefficients are used from Chakraborty and Blagojevic experiments due to time constraints to having to perform another set of project that could be an entirely different thesis project itself. However, the values of coefficients applied are of the same type of PV cell, hence, providing a much closer correlation of results.

The irradiance is a significant factor influencing the discrepancy between $SR_{\text{isc}}$ and $SR_{\text{pmax}}$ of the PV module. For a typical PV module with 100-1100W/m$^2$ irradiance, the short circuit current, $I_{\text{sc}}$ is proportional to the irradiance value. As irradiation of the PV decreases below 1000W/m$^2$, the maximum power of PV reduces faster than the declination of irradiance received by PV module. This results in two values of Soiling Ratio, $SR_{\text{isc}}$ and $SR_{\text{pmax}}$.

$SR_{\text{isc}}$ is significant in cases where the main interest is the effect of soiling on the short circuit current, while $SR_{\text{pmax}}$ is used when the main focus is the to study the effect of soiling on the power output of the PV. In this project, $SR_{\text{pmax}}$ is significant as it relates to the performance of the PV modules from the soiling accumulation.

In order to get the actual magnitude of the soiling impact, the datasheet values of manufactured PV modules are examined for modules under STC (1000W/m$^2$, 25°C) at Normal Operating Cell Temperature (NOCT). Figure 11 above shows the soiling ratio estimated by
examining modules under STC at NOCT (Homer 2018). Soiling ratio measurement of a four day period done by Kimber produces an uncertainty of approximately ±1% (Maehlum 2013).

3.2.3. Effect of Soiling Non-Uniformity

SRsc and SRp, max differences can be significantly large due to the impact of non-uniform soiling across the PV modules. Soiling non-uniformity is considered as a big issue as it results in a more prominent power loss compared to having the same amount of soiling distributed across the PV panel uniformly. Some of the effects leading to soiling non-uniformity are from natural causes, i.e. wind and rain (Quansah et al. 2017).

![Figure 12: Dust accumulation at the bottom edge of the frames (Solar Energy 2008)](image)

Figure 12 above shows the non-uniformity of dust accumulation on the edges of the PV frame. This highlights the common areas of dust accumulation on the PV modules. Dust normally accumulates at the bottom ridge of the PV module frames. The angle of the PV module also affects the dust precipitations. A lower tilt angle PV module would have more dust accumulation and vice versa (Quansah et al. 2017).
3.3 Dust Mitigation Strategies

3.3.1 Natural Dust Removal

Removing dust naturally is related to natural resources of the world. This includes rainwater, gravity and wind power blowing the dust off the Photovoltaic (PV) panel. Natural dust removal methods are not enough in maintaining the cleanliness of the PV panel especially the ones in middle eastern countries where sandstorms are quite common and there is little rain occurring. This is proven by the reduction in performance of the PV modules tested in Riyadh, Saudi Arabia where a PV module’s energy output has been reduced by up to 32% after eight months. (Elminir et al. 2006)

3.3.2 Mechanical Dust Removal

Removing dust by mechanical means involves the use of a machine to drive the dust off the PV panels. Pressurized water, air and brushing the panels with a cloth using windscreen motion are the typical examples of dust removal using a machine. The device can be programmed to execute dust mitigation strategies by using timer based or sensor based coding. Brushing the panels using windscreen motion can be done using a microfibre cloth to avoid damaging the panels. However, this method is inefficient as it has a high potential of scratching the PV modules when wiping or brushing due to friction between dust particles and PV cells. Pressurized water cleaning is also a valid method of removing dust and soiling on the PV panels. Nonetheless, building a PV system with pressurized water cleaning strategy would be very energy consuming. This is due to the presence of a water pump to maintain high pressure of water sprayed onto PV panels. The presence of the pump is essential as it differentiates the natural cleaning of rainwater with the mechanically pressurized water cleaning. Thus, using pressurized water unfortunately comes with the cons where it would be energy consuming, consequently increasing the cost of the project. Besides using water, air
pressure can also be used to clean the PV panels. Nevertheless, this method would also require an air pump, thus causing a rise in project costing.

3.3.3 Hydrophobic Coatings Dust Removal

The self-cleaning coatings can be made of a hydrophobic material. Hydrophobic coating repels water from the PV panels making sure there are no water droplets or watermarks on the PV panel. Examples of these types of surfaces are leaves and lotus plants. Hydrophobic surfaces usually are formed by micro or nanostructure sized surfaces. This enables water droplets coming in contact with the surface to be repelled and rolled off while carrying dust particles. (He, Zhou, and Li 2011)

3.3.4 Electrostatic Dust Removal

Using electrostatic means of removing dust from the PV panel is by a simple electric method. This is a very cost-effective method of self-cleaning the PV panels as it uses low energy for operation. The principle of the operation of electrostatically removing dust from the PV panels is by electric curtains. The electric curtain is when a series of electrodes connecting to the AC supply produces a standing wave field. With the correct frequency and conditions, the excited charged wave field levitates the dust particle, moving it to the edge of the PV panel and eventually cleaning the PV panel (Liu and Marshall 2010).
3.4 Standard Test Conditions Correction Procedure

There are several ways to conduct standard test conditions correction procedures for PV panels output. One can follow the International Electrotechnical Commission (IEC 60891) or the American Society of Testing Material (ASTM E 1036-08) standards. The IEC 60891 has three different correction procedures. The ASTM E 1036-08 has the Blaesser method and the Anderson method. For the purpose of this project, the correction procedure 1 of the IEC 60891, with the following equation is used (International Electrotechnical Commission 2009):

\[ I_2 = I_1 + I_{SC} \left( \frac{G_2}{G_1} - 1 \right) + \alpha (T_2 - T_1) \]

*Equation 4: New corrected current at STC*

\[ V_2 = V_1 - R_S (I_2 - I_1) - k (I_2) (T_2 - T_1) + \beta (T_2 - T_1) \]

*Equation 5: New corrected voltage at STC*

Given:
- \( I \): Current [A]
- \( I_{SC} \): Short circuit current [A]
- \( V \): Voltage [V]
- \( T \): Temperature [°C]
- \( G \): Irradiance [W/m²]
- \( \alpha \): Temperature coefficient representing behaviour of short circuit current [A/°C]
- \( \beta \): Temperature coefficient representing behaviour of open circuit voltage [V/°C]
- \( R_S \): Internal series resistance [Ω]
- \( k \): Curve correction factor [Ω/°C]

Based on the above Equation 4 and Equation 5, subscript “1” represents points measured from the IV curves. Subscript “2” refers to the corrected or desired values. To get the thermal coefficient, a graph with axis \( I_{SC}, V_{OC}, P_{MAX} \) is plotted against the temperature axis. The values of the slope of each graph represents the temperature coefficient of the particular type of PV cell. Tim Blagojevic has done a study on different types of PV technology and different types of correction procedures taken. It has been found out that an amorphous cell has thermal coefficient \( \alpha \) of 0.0001, \( \beta \) of -0.0941, \( R_S \) of 4 and \( k \) of 0.001 (Blagojevic 2016). These values are used for this thesis project.
4. Design specifications and features

Figure 13 above shows the design features of the project. The orange highlighted box are the power supply connection. The power supply connection is according to the voltage input type compatibility of each devices. The blue box is the equipment used to retrieve data. Data retrieval of each equipment are as follow:

- **SD Card**: Dust density and voltage of LDR
- **PROVA**: IV curve of PV modules
- **Solar Survey 200R**: PV temperature, ambient temperature, irradiance and angle of PV elevation

PV elevation angle and direction is kept constant at 32degree facing North.
4.1 Arduino

The Arduino UNO is a compact microcontroller board that has gained interest as part of a hobby and in the professional industry. It can create a program and create an interface between two devices and control devices in a simple manner. Arduino works with a ‘sketch’ software to write and upload the program into the Arduino UNO board. The language being applied to this microcontroller is derived from programming C. The software also enables the user to use built-in fundamental programs that comes with a ‘help’ guidance to help the user, hence making the program user-friendly. The Arduino UNO REV3 SMD Edition is the model used in this thesis project. It is based on a microcontroller board based on an ATmega328. The Arduino UNO REV3 SMD has 14 digital output and input pins of which 6 is a Pulse Width Modulation (PWM) type. It also has 6 analog inputs, a 16MHz crystal oscillator, a power supply jack, USB port, ICSP headers and a reset button (Lahfaoui et al. 2017). Table 3 below shows the specification of the Arduino Uno Rev 3 SMD used in the project.

<table>
<thead>
<tr>
<th>Microcontroller</th>
<th>ATmega328P</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage Output</td>
<td>5V</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>7-12V</td>
</tr>
<tr>
<td>Supply Voltage (Maximum)</td>
<td>6-20V</td>
</tr>
<tr>
<td>Digital Pins</td>
<td>14</td>
</tr>
<tr>
<td>Pwm Digital Pins</td>
<td>6</td>
</tr>
<tr>
<td>Analog Pins</td>
<td>6</td>
</tr>
<tr>
<td>Clock Speed</td>
<td>16 MHz</td>
</tr>
<tr>
<td>Length</td>
<td>68.6 mm</td>
</tr>
<tr>
<td>Width</td>
<td>53.4 mm</td>
</tr>
<tr>
<td>Weight</td>
<td>25 g</td>
</tr>
</tbody>
</table>

*Table 3: Specification for Arduino UNO Rev3 SMD (Lahfaoui et al. 2017)*
4.2 Photovoltaic Panels

An amorphous panel is implemented for the purpose of this experiment. Although crystalline silicon PV cells are mostly known for their high efficiency, the current project uses a thin film cell type of PV. The type of the cell does not really matter in this project as it is merely a proof of concept to study the effect of soiling on PV panels.

For the purpose of this project, an amorphous type of cell is used. At maximum power point, the current is estimated to be at 143mA with 7 volts. The IV curve characteristic of the panel also shows a short circuit current at 150mA and open circuit voltage of 11 volts. Regarding mounting the PV panels, a standard universal procedure is applied. The dimension of the module is quite compact hence, lowering the power output of range from 0.75Watts to 1.25Watts. The specifications of the PV module are as per shown in Table 4 below.

<table>
<thead>
<tr>
<th>Solar panel type</th>
<th>Amorphous</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current at Power Max</td>
<td>143mA</td>
</tr>
<tr>
<td>Voltage at Power Max</td>
<td>7V</td>
</tr>
<tr>
<td>Short Circuit Current</td>
<td>150mA</td>
</tr>
<tr>
<td>Open Circuit Voltage</td>
<td>11V</td>
</tr>
<tr>
<td>Mounting Method</td>
<td>Standard Universal</td>
</tr>
<tr>
<td>DC Voltage</td>
<td>6V</td>
</tr>
<tr>
<td>Power</td>
<td>1W</td>
</tr>
<tr>
<td>Product Length</td>
<td>162mm</td>
</tr>
<tr>
<td>Product Width</td>
<td>162mm</td>
</tr>
<tr>
<td>Product Depth</td>
<td>22mm</td>
</tr>
<tr>
<td>Product Weight</td>
<td>0.65kg</td>
</tr>
</tbody>
</table>

Table 4: Amorphous PV panel specifications (Jaycar 2017)
5. **Project Methodology**

5.1. **Dust Measuring System**

Three PV modules were installed on the roof of the Engineering Building of Murdoch University. Three separate experiments were carried out. Two experiments depend on the dust accumulations across the PV panels. The first test was to study the correlation between dust accumulation and the performance of the PV modules in relation to dust mitigation strategies applied. This experiment involves measuring the Soiling Ratio of the PV modules. The second experiment involves measuring the surrounding air quality and the third test is to study the light transmittance going through a sample glass with dust accumulations. The setup for the system is as per shown in Figure 14 below.

![Figure 14: Dust measuring system](image)

The enclosure box for test 2 is mounted at the back of the PV mounting board. This is to avoid direct sunlight exposure and risk damaging the electrical components inside the enclosure.
5.1.1. PV Performance Testing

There are three different conditions setup for the PV modules. Panel A is regularly washed every Monday, Thursday, and Saturday. Panel B is sprayed with a hydrophobic coating at the beginning of the experiment to study the effectiveness of the coating in mitigating dust. Panel C is however left without any dust mitigation strategies. This is crucial to investigate the effect of dust on PV performances from comparing between all the three PV panels.

Panel A is washed using clean water and microfibre cloth to avoid any scratching on the PV modules. Panel B is sprayed with hydrophobic coating using circular polishing motions as per guidelines from the company. A thin layer of coating is applied. The coating enabled the PV module to act as a self-cleaning PV module. Panel C is without any cleaning or dust mitigation system to compare the performance of dust accumulated PV with the panel A and B. The comparison in PV power output signifies the importance of dust mitigation strategies in the PV industry. Several measurements were taken to analyse the performance of the PV modules undergoing different types of dust mitigation strategies. The measurements made are as per shown in Table 5 below.

<table>
<thead>
<tr>
<th>Measurements</th>
<th>Method/Instruments Involved</th>
</tr>
</thead>
<tbody>
<tr>
<td>IV Curve</td>
<td>PROVA</td>
</tr>
<tr>
<td>Tilt Angle</td>
<td>Solar 200R Analyzer</td>
</tr>
<tr>
<td>Ambient Temperature</td>
<td>Solar 200R Analyzer</td>
</tr>
<tr>
<td>PV Temperature</td>
<td>Solar 200R Analyzer</td>
</tr>
<tr>
<td>Wind Speed</td>
<td>Weather Forecast</td>
</tr>
</tbody>
</table>

*Table 5: PV performance analysis with the methodology applied*
The connection of the PROVA to the PV panels are as shown in Figure 15 below.

The PROVA is used to generate IV curves of the panels and is converted to STC conditions using IEC 60891 correction procedure. The IV curves of the panels depend on the measured irradiance and temperature value. Data taking process is conducted every weekday for two weeks worth of data. The data is measured often to reduce uncertainty and for a much more accurate representation of the effect of dust on PV panels performance. In order for a linear comparison of the PV performance, the IV curve data is converted to Standard Test Conditions (STC). The STC conditions for PV panels are as per Table 6 below.

<table>
<thead>
<tr>
<th>Irradiance</th>
<th>1000 W/m²</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature of PV cell</td>
<td>25°C</td>
</tr>
<tr>
<td>Air Mass</td>
<td>AM1.5</td>
</tr>
</tbody>
</table>

Table 6: Standard Test Conditions of PV

Soiling Ratios are also calculated using Equation 2 and Equation 3 from Chapter 3.2 of this thesis report.
5.1.2. Optical Air Quality Sensor

Air quality data is logged into an SD card mounted on the Arduino data logging shield. The data corresponds to the performance of the PV modules by helping to understand dust accumulation on the PV modules.

![Interface of the Optical Dust Sensor](image)

Figure 16: Interface of the Optical Dust Sensor (Instructables 2017)

Figure 16 above shows the connection of the Optical Dust sensor in order to measure the air quality at the site. The optical dust sensor is connected to a 3.3V power supply. A 220uF capacitor and a 150Ω resistor is used as per suggested in the datasheet of the sensor (Sharp 2017). The blue and yellow wire which are ground pins are connected to the ground of the Arduino Uno pin with a 220uF capacitor.
The connection for the Arduino and the dust sensor is as per shown in Table 7 below.

<table>
<thead>
<tr>
<th>Pins on Dust Sensor</th>
<th>Arduino UNO pins</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>White pin 1 (V_LED)</td>
<td>3.3V</td>
<td>With 150Ω in between</td>
</tr>
<tr>
<td>Blue pin 2 (LED_GRD)</td>
<td>GND</td>
<td>With 220μF in between</td>
</tr>
<tr>
<td>Green pin 3 (LED)</td>
<td>Digital output (D02)</td>
<td>Not applicable</td>
</tr>
<tr>
<td>Yellow pin 4 (S_GRD)</td>
<td>GND</td>
<td>Not applicable</td>
</tr>
<tr>
<td>Blue pin 5 (Vo)</td>
<td>Analog input (A3)</td>
<td>Not applicable</td>
</tr>
<tr>
<td>Red pin 6 (Vcc)</td>
<td>3.3V</td>
<td>Not applicable</td>
</tr>
</tbody>
</table>

Table 7: Connection from Arduino board to the optical dust sensor

Figure 17 below shows the physical wiring inside the enclosure containing the optical dust sensor. The dust sensor is placed outside of the enclosure to ensure a continuous data logging of the dust density. The dust density is derived from the voltage at the digital output, D02 of the Arduino board.

Figure 17: Wiring inside the enclosure
5.1.3. Transmittance of Light

Autocad is used to design the casing for the light transmittance testing. The structure of the design considers the placement for the devices involved for transmittance testing. The few devices involved is a glass to accumulate dust, an LED to produce light and a LDR to analyse the reduction in light transmittance from the LED due to soiling. The finalized design of the casing is as per Figure 18 below:

![Figure 18: Autocad design for light transmittance testing](image)

The design is then 3D printed for glass, LED and photodiode mounting. The finished printed out design is as per Figure 19 below. Figure 17 below also highlights the location of the LDR which is mounted on top of the casing, LED mounted below the casing and a glass in between the two. The LED type used was a 5mm red LED, while the LDR used was an epoxy coated LDR with reference to MPB12C39A datasheet from Wiltronics.

![Figure 19: Position of LED and LDR for light transmittance testing](image)
Figure 20 shows the connection of the LED and LDR to the Arduino Uno. A data logging shield is also mounted on top of the Arduino Uno. The orange cable in figure 18 is an I2C communication between the SDA and SCL to analog input 4 and 5 or the Arduino UNO board. The grey cable is the connection between the LDR1, LDR2, LDR3 with analog input 0, 1 and 2. The cyan cable shows the connection of the digital output of LED1, LED2, LED3 with digital output 8, 7 and 4. The LDR is connected to a 10kΩ resistor while the LED is connected in series with a 270Ω resistor. Each LED can however, withstand a maximum of 20mA current only. Applying Ohm’s law to the circuit, a 270Ω and with a 5V supply, the current going through each LED is calculated to be 18.5mA. Hence a 270Ω resistor is used to prevent the LED from running at a high current rating. The LDR is connected to a 10kΩ resistor as it is about the same value of the resistance of the LDR. Following Ohm’s Law, as the light increases, the resistance of the LDR drops, which in turn increases the current and voltage at analog input A0, A1 and A2.
5.2 Dust Mitigation System

There are numerous ways to mitigate dust and soiling on a PV panel. There are only two methods applied in this project. One is a scheduled washing of the PV modules and another one is a hydrophobic coating on the PV modules. The methodology details of each dust mitigation system applied to the PV module is explained in the next sub-chapter.

5.2.1 Scheduled washing of PV modules

A CL50 glass cleaner is used for cleaning the PV module. The PV module is cleaned every weekday to make sure high power output from PV module A. Figure 21 below shows the cleaning agent used for PV module A.

![Figure 21: CL50 glass cleaner](image)

Besides using CL 50 for scheduled washing of Panel A, CL 50 is also used to prepare the surface of Panel B before the hydrophobic coating is applied.
5.2.2 Hydrophobic coatings

PV module B is coated with hydrophobic layers. A NG-1314/D hydrophobic kit with instructions of application specially made for PV panels is purchased from Nanovations(Nanovations 2017). The kit contains CL50 cleaning agent and a bottle of hydrophobic coating. This can be seen in Figure 22 below.

![Figure 22: Hydrophobic coating NG-1314/D](image)

Before conducting the application, the surface is made sure to be clear of dirt or grime that could cause scratches and reduce the PV performance. The CL 50 cleaning agent is also used to clean the PV panel. Cleaning is started from the top of the PV panel is per recommended in the Application instruction of the NG-1314/D hydrophobic kit provided by Nanovations supplier. The cleaning is conducted in circular motions. After surface preparation is conducted, the application of the hydrophobic coating can begin. Before applying the coating, the surface is made to be thoroughly dry. The application of coating is by spraying a small amount on the PV surface with circular motions using the cloth provided by the Nanovations. A trigger spray head is attached to the bottle and product is applied as thin as possible without leaving any area of PV module B uncoated.
5.3 Arduino Programming

5.3.1 Communication Protocols

**SPI (Serial Peripheral Interface)**

The SPI is a communication protocol used by the Arduino. Digital pin 10, 11, 12 and 13 support SPI communication using the SPI library. Digital pin 10 is the slave select (SS), digital pin 11 is the Master Out-Slave In (MOSI), digital pin 12 is the Master In-Slave Out (MISO), and the digital pin 13 is the Serial Clock (SCK). With the use of an SPI communication protocol, a single master device controls all the other slave devices. A summary of the SPI connection of the Arduino Uno is as shown in Table 8 below.

<table>
<thead>
<tr>
<th>Digital pin</th>
<th>Descriptions</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>SS</td>
<td>Pin used by master to control enabling and disabling peripheral devices. The communication between peripheral devices and master only happens when the pin is set to Low.</td>
</tr>
<tr>
<td>11</td>
<td>MOSI</td>
<td>Transmit data to the slave</td>
</tr>
<tr>
<td>12</td>
<td>MISO</td>
<td>Transmit data to the master</td>
</tr>
<tr>
<td>13</td>
<td>SCK</td>
<td>Clock pulse that synchronizes data transmission.</td>
</tr>
</tbody>
</table>

Table 8: SPI pins on Arduino Uno (Arduino 2017)

Besides the digital pin mentioned, the SPI communication port can also be found on the In-Circuit Serial Programming (ICSP) header as shown in Figure 23 above.
**I²C (Inter-integrated Circuit)**

The I²C communication protocol provides a mean of communication between master (Arduino Uno board) and the slave (other peripheral devices). It is similar to SPI regarding short distance communication between devices. However, an SPI has certain disadvantages, where its connection between a single master and a single slave would use up to four lines. Figure 24 and Figure 25 below shows the difference of wiring between an SPI and an I²C communication protocol wiring. This causes the SPI bus routing signal to be more complex with a large number of wiring compared to I²C wiring. (Sfuptownmaker 2017). The I²C has two wire signals and uses the “wire.h” library for communication.

![Figure 24: SPI communication protocol](Sfuptownmaker 2017)

![Figure 25: I²C communication protocol](Sfuptownmaker 2017)
The two primary signals for I²C are the Data Signal (SDA) and Clock Signal (SCL). The SDA controls the data being sent or received, whereas the SCL controls the speed of data transmission (Aidan 2016). For an Arduino Uno board, the SDA is pin Analog Input 4, while SCL is pin Analog Input 5. Figure 26 below shows orange wiring for the connection for SDA and SCL on the Arduino board.

![Figure 26: SDA and SCL connection on the Arduino Uno board](image)

**Serial Communication**

Serial communication is a standard way of communication between the Arduino and the computer. Digital pulse is transmitted and received at a given speed between the transmitter (Tx) and the receiver (Rx) (Kontopoulous 2012). The Tx and Rx LED can be seen from the Arduino board as per highlighted in Figure 27 below.

![Figure 27: Transmitter and receiver pins for serial communications on the Arduino](image)
5.3.2 Variables

Variable declarations are made to store data. Fundamentals of creating variables are the name of the variable, the type of data that is to be stored and the pin number where data is to be stored. For example, “int LDRPin1 = A0” which tells the Arduino that integer type of data will be stored in variable name LDRPin1 from Analog input 0. The variables declared in this project is as per shown in Table 9 below.

<table>
<thead>
<tr>
<th>Programming</th>
<th>Variable name</th>
<th>Variable Type</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Date and Time</td>
<td>Timestamp</td>
<td>character</td>
<td>20 due to 18 characters used (hh:mm:ss dd/mm/yyyy)</td>
</tr>
<tr>
<td>Data logging</td>
<td>CS_pin</td>
<td>integer</td>
<td>10 – Digital pin set to an output for communication between Arduino and SD card.</td>
</tr>
<tr>
<td></td>
<td>Data</td>
<td>string</td>
<td>To store combined data</td>
</tr>
<tr>
<td>Light transmittance testing using LED and LDR</td>
<td>LDRPin1</td>
<td>integer</td>
<td>A0- Analog Input 0</td>
</tr>
<tr>
<td></td>
<td>LDRPin2</td>
<td>Integer</td>
<td>A1- Analog Input 1</td>
</tr>
<tr>
<td></td>
<td>LDRPin3</td>
<td>Integer</td>
<td>A2- Analog Input 2</td>
</tr>
<tr>
<td></td>
<td>LedPin1</td>
<td>Integer</td>
<td>8 - Digital Output 8</td>
</tr>
<tr>
<td></td>
<td>LedPin2</td>
<td>Integer</td>
<td>7- Digital Output 7</td>
</tr>
<tr>
<td></td>
<td>LedPin3</td>
<td>Integer</td>
<td>4 - Digital output 4</td>
</tr>
<tr>
<td></td>
<td>sensorValue1</td>
<td>integer</td>
<td>Store data at Analog Input 0</td>
</tr>
<tr>
<td></td>
<td>sensorValue2</td>
<td>Integer</td>
<td>Store data at Analog Input 1</td>
</tr>
<tr>
<td></td>
<td>sensorValue3</td>
<td>Integer</td>
<td>Store data at Analog Input 2</td>
</tr>
<tr>
<td></td>
<td>voltLDR1</td>
<td>Float</td>
<td>Store data of LDR1</td>
</tr>
<tr>
<td></td>
<td>voltLDR2</td>
<td>Float</td>
<td>Store data of LDR2</td>
</tr>
<tr>
<td></td>
<td>voltLDR3</td>
<td>Float</td>
<td>Store data of LDR3</td>
</tr>
<tr>
<td>Air quality testing using an optical dust sensor</td>
<td>MeasurePin</td>
<td>Integer</td>
<td>Analog input pin 3</td>
</tr>
<tr>
<td></td>
<td>ledPower</td>
<td>Integer</td>
<td>Digital output 2</td>
</tr>
<tr>
<td></td>
<td>voMeasured</td>
<td>Float</td>
<td>Store raw data of dust</td>
</tr>
<tr>
<td></td>
<td>calcVoltage</td>
<td>Float</td>
<td>Store voltage data of dust</td>
</tr>
<tr>
<td></td>
<td>dustDensity</td>
<td>Float</td>
<td>Store dust density data</td>
</tr>
<tr>
<td></td>
<td>samplingTime</td>
<td>Integer</td>
<td>280us is the wait time before output is measured again</td>
</tr>
<tr>
<td></td>
<td>deltaTime</td>
<td>Integer</td>
<td>40us delay before switching the LED on</td>
</tr>
<tr>
<td></td>
<td>sleepTime</td>
<td>integer</td>
<td>9680us delay after switching LED off</td>
</tr>
</tbody>
</table>

Table 9: Variable declarations
5.3.3 Detailed Program

Library and Variable Declaration

![C++ code snippet]

Figure 28: Libraries used in the Arduino program

Figure 28 above shows the libraries that are used for the program. The Serial Peripheral Interface (SPI) is a serial data protocol used for communication between the Arduino and the SD card. The first library used is in black as it is not a built-in library inside the Arduino sketch. It is an imported real-time clock library created by JeeLabs (JeeLabs 2017).

![Variable declaration code snippet]

Figure 29: Declaration of input and output types and pins

Figure 29 above is to declare the variables pin and data type of the time, chip select, real-time clock (RTC), LED, LDR, dust sensor. Data types such as integers are used when the data is of a whole number, while float is used when data type has decimal points. Char, on the other hand, is an abbreviation for character. It is used to hold numbers from -128 to 127 (Arduino 2017). A string type variable is also declared as ‘Data’ to store the array of data for data logging on the SD card in a later program. “//” is ignored by Arduino as it is only a comment for user for the ease troubleshooting when necessary. Other than variable declarations, the type of RTC used has also been declared. Other than that, there are various types of RTC on the market. The RTC library used specifically for this project is DS1307, hence declared.
**Void setup program**

```cpp
void setup()
{
    // LED- LDR
    pinMode(ledPin1, OUTPUT);
    pinMode(ledPin2, OUTPUT);
    pinMode(ledPin3, OUTPUT);

    // Dust sensor
    pinMode(ledPower, OUTPUT);

    // Chip Select
    pinMode(CS_pin, OUTPUT);

    Serial.begin(9600);
    Wire.begin();
    Serial.println("Initialising Card");

    if (!SD.begin(CS_pin))
    {
        Serial.println("Card Failure");
        return;
    }
    Serial.println("Card Ready");
    rtc.begin();
}
```

*Figure 30: Void setup program*

Figure 30 above shows the void setup section of the program. This part of the program is used to signify output to the LED, LDR and dust sensor. From the Figure 30, program “serial.begin”, “wire.begin” and “SD.begin” which is used to initiate the serial, wire and SD library. “wire.begin” is specifically used to initiate the Inter-Integrated Circuit (I²C) bus as master or slave (Arduino 2017). The I²C bus is used as a communication between the Arduino and the Real Time Clock (RTC). “SD.begin” is used to start the SD card, SD library and initiate the SPI bus and the chip select pins. Besides that, the “serial.begin” is also used to set the data rate in bits per second (baud) for transmission and communication of data (Arduino 2017).
**Void Loop Program**

```c
void loop()
{
}
```

*Figure 31: The start of the void loop program*

The beginning of the void loop program is shown in Figure 31 above. Void loop is the body of the program that repeats the program continuously in a loop. The word void is highlighted in blue as it is only the function declaration type for loop used.

```
// turn the ledPin 1, 2, 3 on
digitalWrite(8, HIGH);
digitalWrite(7, HIGH);
digitalWrite(4, HIGH);

// read the value LDR:
sensorValue1 = analogRead(LDRPin1);
voltLDR1 = sensorValue1*(5/1023.0);
sensorValue2 = analogRead(LDRPin2);
voltLDR2 = sensorValue2*(5/1023.0);
sensorValue3 = analogRead(LDRPin3);
voltLDR3 = sensorValue3*(5/1023.0);
```

*Figure 32: LED and LDR loop program*

LED and LDR program is as per Figure 32 above. The first part of the program is to make sure the LED are on using the “digitalWrite” function. The second part of the program is to read the analog values retrieved by the assigned LDR pins. An equation is also made to convert the raw analog reading to a more meaningful value of voltage. The voltage signifies the reduction in transmittance of light from dust accumulation on the glass. The equation is as per below.

$$V_{\text{oltage component}} = \frac{\text{Raw Value}_{\text{component}} \times \left(\frac{\text{Supply Voltage}}{1023}\right)}$$

*Equation 6: Voltage calculation based on raw value from Arduino*

Arduino consists of 10-bit resolution for digital inputs. The Arduino yields a reading of 5V with 10 bits resolution, having 1024 units starting from 0 to 1023. Hence, the supply voltage used is 5V and are mapped to a 1023 integer output.
Based on Figure 33 above, real-time is used to map the data logging of the collected data to its corresponding period. A variable called “Timestamp” is made to store the value of time. “Serial.sprintf” is a command used to display the time stamp for monitoring purposes during program testing.

```cpp
//TIME
DateTime now = rtc.now();
strftime("%d/%m/%Y %H:%M:%S", &now, "%d/%m/%Y %H:%M:%S", now.hour(), now.minute(), now.second(), now.day(), now.month(), now.year());
Serial.print(Timestamp);
```

**Figure 33: Setting the time for the RTC**

Figure 34 is the code used to display the LDR output, turn on the dust sensor and read the value of the dust sensor in raw signal, calculated voltage and dust density. The calculated voltage is based on Equation 6 of this chapter. The dust density is based on an equation derived from Chris Nafis (Nafis 2017). The dust density is based on a raw value from the analog pin of the Arduino. An equation as per Figure 34 calculates the voltage and the converts the voltage into dust density. Based on calculation, a positive dust density is only possible when the raw value is above 183, which is equivalent to a voltage of 0.59V. Based on this test, the values of the highest voltage is 0.35, which shows that the dust density is very minimal and proves that the air is clean at the time of the experiment.

```cpp
//LDR-LDR
Serial.print("", LDR(V):"); // linear equation taken from http://we
Serial.print(voltLDR1); // Chris Nafis (c) 2012
dustDensity = 0.17 * calcVoltage - 0.1;
Serial.print(" Raw Signal: ");
Serial.print(voltageMeasured);
Serial.print(" ");
Serial.print(" Voltage: ");
Serial.print(calcVoltage);
Serial.print(" ");
Serial.print(" Dust Density: ");
Serial.printIn(dustDensity);
Serial.print(" ");
```

**Figure 34: Program to display the analog input and digital output**
A new variable called “Data” is created to store combined array of data in a string format to be stored inside the SD card. This can be shown in Figure 35 above.

```java
//SD
File dataFile = SD.open("datalog.csv", FILE_WRITE);
if (dataFile)
{
    dataFile.println(Data);
    dataFile.close();
}
else
{
    Serial.println("Couldn't open log file");
}
//SD
delay(60000);
```

Figure 36 above shows how a document type .csv is created for data logging. ‘SD.open(“datalog.csv”, FILE_WRITE)’ syntax is used to open the SD card for writing into the .csv file created. This creates a .csv file on the SD card for data logging purposes. Besides that, based on the figure above, a ‘delay’ function is used. The ‘delay()’ function is in milliseconds by default. Thus, to get a 1 minute delay, 1 minute is converted to milliseconds. A time delay of 60000 milliseconds, which is equivalent to 1 minute, is programmed to make sure data is taken every minute. Dust density’s data was every 1 minute. The data are analysed and an average of the 24hours of the day starting from 3rd November 2017 to 20th November is used to describe the air quality of that particular day in relation to the power output of the PV modules. Transmittance data however is sampled throughout the same date duration. However, the data are filtered to only analyse the data during night time from 9pm to 12pm to prevent external sunlight affecting the accuracy of the data.
6 Results and Discussions

6.1 Climate during Experiment

Figure 37 below shows the climate conditions in Perth around 3rd November 2017 to 20th November 2017. This data is significant in correlation to the variance in PV performance. The data were taken from Murdoch University Weather Station (Murdoch University & Alcoa Inc 2017). The PV modules perform best when the wind speed and the humidity are high. Wind speed can affect the PV performance by blowing off the dust from the PV panel, thus providing a cleaner panel and a higher PV power output. Based on the figure above, the highest humidity is on the 17th of November. The humidity percentage shows how the weather is on that particular day. This shows that the day is rather cloudy or rainy compared to other days with low humidity. Rainwater has drastic effects on the PV panels as it naturally cleans the PV panels. On the 17th November, there was a drizzle of rain in the morning. With high humidity, it is easier to wash away the soiling adhering to the PV panel. Hence, resulting in a slight increase in power output of each panel on the following day in comparison to the previous day.
6.2 Correction procedure of the IV Curve of the PV

Figure 38 above shows a sample of the difference in IV curve before and after correction is applied. Thermal coefficient $\alpha$ of 0.0001, $\beta$ of -0.0941, $R_s$ of 4 and $k$ of 0.001 from Tim Blagojevic is being implemented in deriving the STC IV curve (Blagojevic 2016). A summary of the values used is summarized in Table 10 below:

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal coefficient, $\alpha$</td>
<td>0.0001</td>
</tr>
<tr>
<td>Thermal coefficient, $\beta$</td>
<td>-0.0941</td>
</tr>
<tr>
<td>Series resistance, $R_s$</td>
<td>4</td>
</tr>
<tr>
<td>Correction factor, $k$</td>
<td>0.001</td>
</tr>
</tbody>
</table>

*Table 10: Parameters used for correction to STC*

The IV Curve in Figure 38 is a sample of how data is corrected based on real-time data from PROVA on the 8th of November 2017. The graph shows an increment in maximum voltage from 8.11V to 10.41V. The short circuit current, $I_{sc}$ increases from 0.1386A to 0.1461A and the open circuit voltage, $V_{oc}$ increases from 10.251V to 12.61V.
Standardizing the values of irradiance and temperature back to its STC enables users to compare PV performance. PV performance comparison for this particular project is to compare the difference in power output different panels with different dust mitigation strategies.

![Corrected to STC Power Curve](image)

**Figure 39: Comparison of Power Curve before and after correction to STC**

The power curve from Figure 39 above shows the difference in maximum power between before and after correction procedures have been implemented. With a corrected to STC curve, the irradiance is higher and the temperature is lower hence, signifying a higher yield of power output. The maximum power for this power curve is at 1.173W.
6.3 PV Performance

6.3.1 Panel A

Figure 40: Panel A before and after 2 weeks of dust mitigation

Figure 40 above shows the before and after of 2 weeks of dust deposition with the dust mitigation strategies applied. For this panel, the dust mitigation strategy is the best method as it is washed every day for the best PV performance result.

In terms of performance analysis, panel A has a maximum power of 1.283W on day 1 of the test, 3rd November 2017.

A summary of the analysis made on the day of the maximum power is as per below:

- Short circuit current, $I_{SC} : 0.169A$
- Open circuit voltage, $V_{OC} : 11.037V$
- Fill factor, $FF : 0.756$
- Wind speed, $ws : 19m/s$
- Humidity : 51%

The soiling ratio, $SR_{PMax}$ is 0.46 as per Equation 2. A soiling ratio of 1 signifies that the module is clean without any dust. The soiling ratio for panel A is the closest to 1 hence, proving that the panel is most clean in comparison to the other two panels.
Based on Figure 41 above, the average of power out coming from a scheduled washing PV panel is 1.16W which is the highest power output compared to the other two panels which will be discussed in a later section of this thesis. The highest power output of Panel A is at day one of the experiment with a 1.28W power output. Panel A has a minimum power output of 0.888W, which is at the last day of the experiment on the 20th November 2017. The power output of the panel shows an overall decreasing trend throughout the experimental duration. This is due to dust accumulation on the PV panel. Figure 41 above shows a decrement trend of the graph with sudden uprises on certain days due to climate conditions helping to clean the PV modules naturally. The decrease in $P_{\text{MAX}}$ can also be due to degradation of the PV module as time passes by(Bouraiou et al. 2018).

Figure 41: Panel A performance
6.3.2 Panel B

Figure 42 above shows the soiling accumulation on top of PV Panel B. Panel B has hydrophobic coating on it that helps repel soiling or dust as a dust mitigation strategy. The performance of Panel B is best on the 3rd November 2017 with 1.324W, day 1 of the test.

A summary of the analysis made on the day of the maximum power is as per below:

- Short circuit current, $I_{SC}$ : 0.136A
- Open circuit voltage, $V_{OC}$ : 12.87V
- Fill factor, FF : 0.731
- Wind speed, $w_s$ : 19m/s
- Humidity : 51%

The soiling ratio, $SR_{P_{MAX}}$ on the other hand is 0.27 as per Equation 2. A soiling ratio of 1 signifies that the module is clean without any dust. The soiling ratio for panel B is the furthest from 1 in comparison to panel A and C hence, proving that the panel is very dirty.
Panel B is performing at its best on the first day due to no dust accumulation. Dust starts to accumulate on panel B as day goes by. Panel B has the highest soiling ratio compared to other panels. This can be seen in Figure 43 where the panel is dusty after two weeks being left on the site with hydrophobic coating on. Figure 43 above shows the overall trend of Panel B throughout the data taking process. Panel B also shows an overall downward trend of the power maximum with several peaks. The downward trend is expected as PV panel degrades over time.

Panel B also produces an average of 1.129W power output which is slightly lower than panel A for about 3%. This highlights the benefit of scheduled washing the PV panel for the best results of performance.
6.3.3 Panel C

Figure 41 above shows the soiling accumulation on top of PV Panel C. Panel C has no dust mitigation strategy applied. However, the performance of Panel C is best on the day one of the experiment, 3\textsuperscript{rd} November 2017 with a maximum power of 1.064W.

A summary of the analysis made on the day of the maximum power is as per below:

- Short circuit current, $I_{SC}$ : 0.120A
- Open circuit voltage, $V_{OC}$ : 12.53V
- Fill factor, $FF$ : 0.705
- Wind speed, $ws$ : 19m/s
- Humidity : 51%

The soiling ratio, $SR_{P_{MAX}}$ is 0.35 as per Equation 2. A soiling ratio of 1 signifies that the module is clean without any dust. The soiling ratio for panel C is the between the soiling ratio on panel A and B. This shows that a panel without any dust mitigation has lower dust accumulation. This may be due to non uniform application of hydrophobic coating.

Figure 44: Panel C before and after 2 weeks of dust mitigation
Figure 45 above shows the overall trend of Panel C throughout the data taking process. Panel C also indicates an overall downward trend of the power maximum with several peaks. The downward trend is expected as PV panel degrades over time. Delamination is also present on the PV panel. This is highlighted in Figure 45.

Panel C is performing at its best on the first day due to no dust accumulation. Dust starts to accumulate on panel C as day goes by. Panel C has the medium soiling ratio. This can be seen in Figure 44 where the panel is dusty after two weeks being left on the site with no dust mitigation applied. Panel C has an average power of 0.92W which is lower than panel A for approximately 21%. This highlights the drastic effect of soiling and signifies the significance of self-cleaning PV in the PV industry.

Regarding light transmittance test, a clean glass panel gives out a voltage reading of 0.37V which corresponds to 100% transmittance as of 3rd November. Using ratio as part of the calculation for light transmittance, through the glass after two weeks of dust deposition which is on the 20th November, the voltage output is 0.19V. This corresponds to a 78% transmittance. Which shows a reduction in light transmittance of about 22%.
Based on Figure 46 above, the power output of panel A and B is slightly similar as both panels has dust mitigation strategies applied. The apparent low performing PV panel would be Panel C that is left outside for dust accumulation without any dust mitigation strategies. Panel B yields the highest power output on the 3rd of November 2017. However, if comparing the panel’s average power output throughout a range of days, Panel A produces the highest average power at 1.16W, followed by Panel B with 1.12W and then Panel C with 0.92W. This shows that there is a significant difference in reduction of performance between a panel that has dust mitigation strategies and the ones without. Soiling without dust mitigation strategies is a big challenge to PV industry as it causes as high as 20.6% reduction in average power output if being compared to a clean Panel A that is regularly washed. This reduction in PV performance is based on an 18 days dust accumulation in Murdoch University, Perth, Western Australia during summer.
Figure 47: Decrement in performance of PV modules

Figure 47 shows the decrement in trend of all module performance. The decline in power output is related to soiling on the PV panel. This is an 18 days duration experiment. As seen in the figure above, the decrement from day 1 to day 18 of panel A is 30.8%, while for panel B is 47.4% and panel C is 31.4%. As a conclusion, scheduled washing seems to be the best way to prevent soiling effect on the PV performance.

In a short timeframe of 18 days, the PV panel’s performance has significantly decreased. 22g/m² soiling could effect a reduction in PV module efficiency up to 26% (Jiang, Lu and Sun 2011). Using ratio from Jiang’s article in 2011, the estimated mass of soiling on top of the PV module for the weeks duration on Panel C is 26.56 g/m². Panel B and C has a slight difference in PV performance output. Panel B performs 16% worse than Panel C. There is a small amount of increase in performance of panel A which has been washed daily compared panel C which performs 0.6% better. This signifies the need for PV washing as the hydrophobic coating has not been really effective in mitigating dust from the PV panels.
Figure 48 shows the condition of all the PV modules after being exposed to dust deposition with dust mitigation strategies applied. From the left of Figure 48, panel A is the cleanest due to scheduled washing dust mitigation. The middle PV panel is Panel B where a hydrophobic coating is applied earlier of the experiment. Panel B has the most apparent soiling on top of the module. Panel C which has no dust mitigation has a few soiling and some bird droppings.
7 Problems Encountered and Countermeasures

7.1 Power Supply

The first problem encountered is a loss of data due to battery supply depletion. A countermeasure for this problem is to change the direct current (DC) supply to a more continuous ongoing supply, alternating current (AC) supply. Figure 49 above shows the change in connection from a DC supply to an AC supply.

7.2 Weatherproof Conditions on Electrical Wirings

Figure 50 above shows the mounting of the electrical wiring enclosure. It is mounted at the back of the PV mounting board to deflect from direct sunlight which could overheat, thus causing damage to the electrical components and rainwater which could cause short circuit in the wiring connection.
Conclusion and Future Works

8.1 Project Conclusion

In conclusion to the objectives and aim, the study of the effect of soiling on the PV performance was a success. It has been proven that soiling has caused a significant reduction in PV performance as per mentioned by Jiang in an article in 2011 (Jiang, Lu, and Sun 2011).

To conclude the first part of the thesis which is PV performance analysis, scheduled washing is the best performing PV panel. Washing the PV modules is the best performing PV panel in terms of power output in comparison to the other two tested panels. All three panels has a reduction in PV performance which can be caused by soiling and degradation. The experiment was conducted over a period of 18 days.

The second part of the thesis was the study of air quality in relation to the PV performance. The air quality in the conducted area, Murdoch University cannot be measured as the dust sensor used was below the detection levels. A higher sensitivity of dust sensor should be used in the future for better results.

The third part of the thesis was the study of light transmittance on a float, low iron glass with dust accumulation. This part of the thesis uses the same type of glass used on the PV modules. A simulation of a separate experiment is conducted and to conclude the results for the two weeks duration of experiment, the light transmittance of the glass left bare without being cleaned or hydrophobic coating has decreased by about 22%. This shows that with an 18 days period of dust accumulation, the PV modules has experienced a reduction in transmittance for quite a significant amount. This correlates to the reduction in PV performance.

As an overall conclusion, soiling greatly affects PV performance. Regarding mitigating dust, there are several methods available. Washing the PV modules is the best dust mitigation
method with a 16.6% difference in performance between a washed module and one with hydrophobic coating applied.

8.2 Future Work Recommendations

Future works can be implemented in this project. Replacing the optical dust sensor with a dust sensor from NOVA SDS011 could provide a more accurate value of air quality in the air. The sensor has a higher sensitivity, detecting particles smaller than the SHARP dust sensor used in this project.

Another recommendation that can be applied is to perform automatic washing on the PV modules. This can eliminate manpower cost in washing the PV modules if being applied to a bigger scale project.

Other than that, the project could be improved by increasing the reproducibility of the data. This can be done by adding more PV modules for each experiment and getting the average performance of the PV modules for a much higher accuracy data. With a bigger scale project, a Distributed Control System (DCS) can also be implemented to ease operator in retrieving information on the PV performance and controlling the automatic washing of the PV modules when necessary.

Longer sample periods can also be made to increase the accuracy of the data. This can be done throughout the year. From a year data collection, the data could be analysed in more depth at every seasons of the year and its effect on soiling of the PV modules.
9 References


10 Appendices

10.1 Appendix A: Calculation for Soiling Ratio

Figure 51: Soiling Ratio Calculation

Figure 51 shows the spreadsheet used to calculate the soiling ratio of the module. The difference in value of $SR_{isc}$ and $SR_{P_{MAX}}$ is due to uneven soiling on the module. The value of the SR are highlighted in red. Top section of the figure shows the values used as an input to the equation for $SR_{isc}$ and $SR_{P_{MAX}}$ calculations.
10.2. Appendix B: Data logging from Arduino Programming Sample

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>E</th>
<th>F</th>
<th>G</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timestamp</td>
<td>Time</td>
<td>LDR1</td>
<td>LDR2</td>
<td>LDR3</td>
<td>Raw dust</td>
<td>calcVolt</td>
</tr>
<tr>
<td>2</td>
<td>10/11/2017 6:00</td>
<td>12:00:23 AM</td>
<td>1.26</td>
<td>0.46</td>
<td>0.33</td>
<td>42</td>
</tr>
<tr>
<td>3</td>
<td>10/11/2017 6:00</td>
<td>12:01:23 AM</td>
<td>1.27</td>
<td>0.46</td>
<td>0.32</td>
<td>43</td>
</tr>
<tr>
<td>4</td>
<td>10/11/2017 6:00</td>
<td>12:02:23 AM</td>
<td>1.26</td>
<td>0.45</td>
<td>0.33</td>
<td>0</td>
</tr>
<tr>
<td>5</td>
<td>10/11/2017 6:00</td>
<td>12:03:23 AM</td>
<td>1.27</td>
<td>0.45</td>
<td>0.32</td>
<td>32</td>
</tr>
<tr>
<td>6</td>
<td>10/11/2017 6:00</td>
<td>12:04:23 AM</td>
<td>1.27</td>
<td>0.46</td>
<td>0.33</td>
<td>18</td>
</tr>
<tr>
<td>7</td>
<td>10/11/2017 6:00</td>
<td>12:05:23 AM</td>
<td>1.27</td>
<td>0.46</td>
<td>0.33</td>
<td>9</td>
</tr>
<tr>
<td>8</td>
<td>10/11/2017 6:00</td>
<td>12:06:24 AM</td>
<td>1.27</td>
<td>0.45</td>
<td>0.32</td>
<td>40</td>
</tr>
<tr>
<td>9</td>
<td>10/11/2017 6:00</td>
<td>12:07:24 AM</td>
<td>1.27</td>
<td>0.45</td>
<td>0.32</td>
<td>31</td>
</tr>
<tr>
<td>10</td>
<td>10/11/2017 6:00</td>
<td>12:08:24 AM</td>
<td>1.27</td>
<td>0.45</td>
<td>0.32</td>
<td>6</td>
</tr>
<tr>
<td>11</td>
<td>10/11/2017 6:00</td>
<td>12:09:24 AM</td>
<td>1.27</td>
<td>0.45</td>
<td>0.33</td>
<td>54</td>
</tr>
<tr>
<td>12</td>
<td>10/11/2017 6:00</td>
<td>12:10:24 AM</td>
<td>1.27</td>
<td>0.46</td>
<td>0.33</td>
<td>12</td>
</tr>
<tr>
<td>13</td>
<td>10/11/2017 6:00</td>
<td>12:11:24 AM</td>
<td>1.27</td>
<td>0.45</td>
<td>0.32</td>
<td>0</td>
</tr>
<tr>
<td>14</td>
<td>10/11/2017 6:00</td>
<td>12:12:24 AM</td>
<td>1.27</td>
<td>0.46</td>
<td>0.32</td>
<td>34</td>
</tr>
<tr>
<td>15</td>
<td>10/11/2017 6:00</td>
<td>12:13:24 AM</td>
<td>1.27</td>
<td>0.46</td>
<td>0.33</td>
<td>15</td>
</tr>
<tr>
<td>16</td>
<td>10/11/2017 6:00</td>
<td>12:14:24 AM</td>
<td>1.27</td>
<td>0.45</td>
<td>0.32</td>
<td>10</td>
</tr>
<tr>
<td>17</td>
<td>10/11/2017 6:00</td>
<td>12:15:24 AM</td>
<td>1.26</td>
<td>0.46</td>
<td>0.33</td>
<td>35</td>
</tr>
<tr>
<td>18</td>
<td>10/11/2017 6:00</td>
<td>12:16:24 AM</td>
<td>1.26</td>
<td>0.45</td>
<td>0.32</td>
<td>59</td>
</tr>
<tr>
<td>19</td>
<td>10/11/2017 6:00</td>
<td>12:17:24 AM</td>
<td>1.25</td>
<td>0.45</td>
<td>0.31</td>
<td>44</td>
</tr>
<tr>
<td>20</td>
<td>10/11/2017 6:00</td>
<td>12:18:24 AM</td>
<td>1.26</td>
<td>0.46</td>
<td>0.33</td>
<td>20</td>
</tr>
<tr>
<td>21</td>
<td>10/11/2017 6:00</td>
<td>12:19:24 AM</td>
<td>1.26</td>
<td>0.45</td>
<td>0.32</td>
<td>37</td>
</tr>
<tr>
<td>22</td>
<td>10/11/2017 6:00</td>
<td>12:20:24 AM</td>
<td>1.27</td>
<td>0.46</td>
<td>0.33</td>
<td>21</td>
</tr>
<tr>
<td>23</td>
<td>10/11/2017 6:00</td>
<td>12:21:24 AM</td>
<td>1.26</td>
<td>0.45</td>
<td>0.33</td>
<td>15</td>
</tr>
</tbody>
</table>

Figure 52 above shows the data retrieved from the SD card for test 2; air quality test and test 3; light transmittance test. The column “LDR1”, “LDR2”, “LDR3” shows the data for test 3 while the column labelled as “Raw dust” and “calcVolt” shows the data for test 2. For test 2, the raw data from the Arduino is converted to a voltage value. The voltage value is then converted to a percentage value of dust density in the air. For test 3, the relevant data is only during night time where there are no external sunlight effecting the LDR voltage reading. The data for all three LDR are then averaged out to get a more accurate representation of the effect of soiling towards the voltage of the LDR.