SILICON NANOWIRES
FOR PHOTOVOLTAIC
APPLICATIONS

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BSc (Hons)

This thesis is presented for the degree of Doctor of
Philosophy of Murdoch University 2008.
I declare that this thesis is my own account of my research and contains as its main content work which has not previously been submitted for a degree at any tertiary education institution.

......................................................

David Adam Parlevliet
Abstract

Silicon nanowires are a nanostructure consisting of elongated crystals of silicon. Like many nanostructures, silicon nanowires have properties that change with size. In particular, silicon nanowires have a band-gap that is tuneable with the diameter of the nanowire. They tend to absorb a large portion of the light incident upon them and they form a highly textured surface when grown on an otherwise flat substrate. These properties indicate silicon nanowires are good candidates for use in solar cells.

Nanostructured silicon, in the form of nanocrystalline silicon, has been used to produce thin film solar cells. Solar cells produced using silicon nanowires could combine the properties of the silicon nanowires with the low material costs and good stability of nanocrystalline based solar cells.

This thesis describes the process of optimisation of silicon nanowire growth on a plasma enhanced chemical vapour deposition system. This optimised growth of silicon nanowires is then used to demonstrate a prototype solar cell using silicon nanowires and amorphous silicon. Several steps had to be accomplished to reach this goal.

The growth of silicon nanowires was optimised through a number of steps to produce a high density film covering a substrate. Developments were made to the standard deposition technique and it was found that by using pulsed plasma enhanced chemical vapour deposition the density of nanowire growth could be improved. Of a range of catalysts trialled, gold and tin were found to be the most effective catalysts for the growth of silicon nanowires. A range of substrates was investigated and the nanowires were found to grow with high density on transparent conductive oxide coated glass substrates, which would allow
light to reach the nanowires when they were used as part of a solar cell. The silicon nanowires were combined with doped and intrinsic amorphous silicon layers with the aim to create thin film photovoltaic devices. Several device designs using silicon nanowires were investigated. The variant that showed the highest efficiency used doped silicon nanowires as a p-layer which was coated with intrinsic and n-type amorphous silicon.

By the characterisation and optimisation of the silicon nanowires, a prototype silicon nanowire solar cell was produced. The analysis of these prototype thin film devices, and the nanowires themselves, indicated that silicon nanowires are a promising material for photovoltaic applications.
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<td>AFM</td>
<td>Atomic Force Microscope</td>
</tr>
<tr>
<td>ATO</td>
<td>Aluminium Tin Oxide</td>
</tr>
<tr>
<td>a-Si</td>
<td>Amorphous Silicon</td>
</tr>
<tr>
<td>a-Si:H</td>
<td>Hydrogenated Amorphous Silicon</td>
</tr>
<tr>
<td>BSE</td>
<td>Back Scattered Electron</td>
</tr>
<tr>
<td>c-Si</td>
<td>Crystalline Silicon</td>
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<tr>
<td>CPM</td>
<td>Constant Photocurrent Method</td>
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<tr>
<td>CVD</td>
<td>Chemical Vapour Deposition</td>
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<tr>
<td>DLTS</td>
<td>Deep Level Transient Spectroscopy</td>
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<tr>
<td>EBSD</td>
<td>Electron Backscattering Diffraction</td>
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<td>Hot Wire Chemical Vapour Deposition</td>
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<td>Indium Tin Oxide</td>
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<td>Nanowire</td>
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<td>OAG</td>
<td>Oxide Assisted Growth</td>
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<td>PECVD</td>
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<td>Pulsed Plasma Enhanced Chemical Vapour Deposition</td>
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<td>QCM</td>
<td>Quartz Crystal Microbalance</td>
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<td>QTS</td>
<td>Charge Transient Spectroscopy</td>
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<tr>
<td>RF</td>
<td>Radio Frequency</td>
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<tr>
<td>SiNW</td>
<td>Silicon Nanowire</td>
</tr>
<tr>
<td>SLS</td>
<td>Solid Liquid Solid</td>
</tr>
<tr>
<td>SOI</td>
<td>Silicon on Insulator</td>
</tr>
<tr>
<td>SPM</td>
<td>Scanning Probe Microscopy</td>
</tr>
<tr>
<td>STM</td>
<td>Scanning Tunnelling Microscope</td>
</tr>
<tr>
<td>STS</td>
<td>Scanning Tunnelling Spectroscopy</td>
</tr>
<tr>
<td>SWE</td>
<td>Staebler Wronski Effect</td>
</tr>
<tr>
<td>TCO</td>
<td>Transparent Conducting Oxide</td>
</tr>
<tr>
<td>TEM</td>
<td>Transmission Electron Microscope</td>
</tr>
<tr>
<td>UHV</td>
<td>Ultra High Vacuum</td>
</tr>
<tr>
<td>VLS</td>
<td>Vapour Liquid Solid</td>
</tr>
<tr>
<td>VHF-PECVD</td>
<td>Very High Frequency Plasma Enhanced Chemical Vapour Deposition</td>
</tr>
<tr>
<td>XPS</td>
<td>X-ray Photoelectron Spectroscopy</td>
</tr>
<tr>
<td>µc-Si</td>
<td>Microcrystalline Silicon</td>
</tr>
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Publications


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CHAPTER 1: INTRODUCTION

1.1 Background Information
Recently there has been a great deal of interest in the fabrication of semiconductor nanomaterials and nanostructures. These are structures or objects with dimensions on the nanoscale. One of the main reasons for this interest is that nanomaterials tend to have properties that differ from those of the bulk material. These properties, such as the large surface area of nanomaterials, can be exploited for various uses. Silicon-based nanostructures are attracting interest as the techniques used to produce them are largely compatible with existing semiconductor fabrication processes. Silicon nanostructures also have properties that differ from those of bulk silicon, such as a band-gap that is tuneable by the size of the structure, which are of interest when producing semiconductor devices.

One silicon nanostructure is nanocrystalline silicon, which structurally consists of a series of nanometre-sized crystallites embedded in a matrix of amorphous silicon material. This material can be used in thin film solar cells (Yue et al., 2006), the properties of which differ from crystalline and amorphous silicon based solar cells. Development of nanocrystalline semiconductor devices is a new and rapidly growing field of research (Cabarrocas, 2004).

The use of nanostructures in solar cells has several advantages over crystalline devices and amorphous thin films, including lower production costs, increased conversion efficiency and improved stability. Nanocrystalline silicon solar cells are predominantly produced as thin film devices ~500nm thick, not including the substrate upon which they are grown. The production of these thin film devices uses much less material than crystalline-based devices allowing lower production costs than those for crystalline silicon solar cells (Green, 2004). Nanocrystalline silicon based solar cells, although having lower conversion efficiencies than crystalline solar cells, potentially have a higher efficiency than their amorphous counterparts.
Thin film amorphous silicon solar cells have a tendency to degrade in efficiency when exposed to light. This is known as the Staebler Wronski Effect (SWE). Nanocrystalline silicon solar cells degrade differently to amorphous silicon solar cells under illumination (Yue et al., 2005) and similar sized microcrystalline devices (Meier et al., 1994) are not as susceptible to the SWE. Nanocrystalline photovoltaic devices undergo only slight photodegradation (6.4%) (Yue et al., 2006). These properties of nanocrystalline solar cells indicate that silicon nanostructures can take advantage of properties of crystalline silicon, such as high efficiency and good stability, as well as the advantages of thin film devices which include low production costs and the ability to coat a variety of substrates.

Creating higher efficiency solar cells is the focus of much research effort. By producing higher efficiency solar cells, or producing efficient solar cells cheaply, the use of solar cells as an alternative energy source becomes more favourable. In an era of rising oil prices and great concern about the environmental impact of coal, oil-fired or nuclear power plants, the hunt is on for clean alternative energy sources. The use of silicon nanostructures would potentially allow for the reduced production and material costs associated with thin film photovoltaics while maintaining the higher efficiency and stability that are characteristic of crystalline solar cells.

A silicon nanowire is an elongated single crystal of silicon with a diameter of tens, to a few hundreds of nanometres and with a length of several micrometres. Silicon nanowires have been the focus of much recent interest due to their unique properties which often differ significantly from bulk silicon (Ma et al., 2003). The electronic band-gap of silicon nanowires is tuneable with the adjustment of the nanowire diameter. The band-gap is known to increase as the diameter of the nanowire is decreased (Ma et al., 2003, Scheel et al., 2005). It has been shown that bulk silicon nanowires combust when a strong light is applied to the sample due to an enhanced photothermal effect (Wang et al., 2003) which indicates a high degree of
absorbance of light. Both of these properties would be of interest when producing solar cells. Controlling the band-gap allows the ability to tune the spectrum of light absorbed by the device. As a solar cell generates power by absorbing light, the demonstrated band-gap tuning and high absorbance bodes well for the use of silicon nanowires in solar cells. Recent results show that silicon nanowires can be used as anti-reflective coatings on crystalline solar cells (Peng et al., 2005). Peng and co-workers’ (2005) top down fabrication technique used a crystalline silicon solar cell as the initial material, the fabrication of which would have involved the high material and processing costs to which crystalline devices are prone. The additional nanowire fabrication step adds more complexity to the fabrication process. An alternative, thin film, approach to the production of silicon nanowire-based devices would maintain the low production costs associated with amorphous silicon and nanocrystalline silicon solar cells. These thin film devices could be grown from the bottom up by various chemical vapour deposition techniques which would allow lower production costs to be maintained while producing a similar material. There has been some mention of silicon nanowire photovoltaics within the literature where nanowires are used as anti-reflective coatings (Peng et al., 2005) or individual solar cells (Tian et al., 2007). However, to date there has been little work done on incorporating silicon nanowires into thin film devices.

The use of silicon nanowires for photovoltaic applications, as solar cells, has great potential due to the proven track record of nanocrystalline-based solar cells and the previously shown high absorbance of light by silicon nanowires (Wang et al., 2003). Silicon nanowires have been produced by chemical vapour deposition and plasma enhanced chemical vapour deposition which are often used to produce amorphous silicon. This indicates that a system designed to produce amorphous silicon could be readily adapted to produce silicon nanowires with minimal modification and/or cost. Thus it would be of great interest to produce solar cells incorporating silicon nanowires into their design to take advantage of the properties of these
Chapter 1: Introduction

silicon nanowires to improve the efficiency of the solar cell, without overly increasing cost of production.

1.2 Scope of the Project
This project aims to produce silicon thin film photovoltaic devices using silicon nanowires. To produce a silicon nanowire based solar cell several steps must be taken. Each step is dependant on, utilises and builds on the information found in the previous step. This methodology is reflected in the experimental approach. The first phase of this project is to produce silicon nanowires in a controlled fashion by Chemical Vapour Deposition (CVD), Plasma Enhanced Chemical Vapour Deposition (PECVD) or other variants of the CVD technique. The growth of silicon nanowires is sensitive to a number of variables including system pressure, substrate temperature and the presence of a gas plasma. This project seeks to optimise these variables for the existing deposition system at Murdoch University, to the level where nanowires can be reliably grown. There is a great deal of information in the open literature regarding the affect of these variables on the growth of silicon nanowires. However, the optimisation of these variables needs to be done for the available system due to the differences in the design of various deposition systems.

Several growth mechanisms are used to describe the growth of silicon nanowires. The most widely used of these is the Vapour Liquid Solid (VLS) mechanism. This was first proposed by Wagner and Ellis in 1964 and uses a liquid metal catalyst to aid the growth. Gold is the catalyst most frequently used although some other catalysts, such as titanium, have also been used. Several different catalysts are trialled as part of this work with the aim of producing silicon nanowires in appropriate numbers for use in photovoltaic devices at lower cost, lower temperatures or higher densities than the conventional gold catalyst.
PECVD has long been used to produce amorphous silicon at high deposition rates and is now also being used to produce microcrystalline (µc-Si) and nanocrystalline (nc-Si) silicon. The use of a gas plasma has also been shown to grow silicon nanowires at a greater rate than CVD (Hofmann et al., 2003). A variant of PECVD that has been used to deposit amorphous silicon at greater rates than PECVD is known as Pulsed PECVD (Das et al., 2003). This variant involves rapidly turning the plasma on and off during the deposition. It follows that this technique may increase the deposition rate of silicon nanowires and this was yet to be investigated. In this project, PPECVD is investigated as a means to improve silicon nanowire growth.

The morphology of silicon nanowires is affected by the substrate on which they are grown. Nanowires are commonly deposited on crystalline silicon substrates as they can provide a source of silicon for the growth of the nanowires and a crystal structure upon which epitaxial growth can take place. Silicon nanowires have been grown on crystalline silicon substrates of various orientations to change the preferred growth direction of the nanowire relative to the surface of the substrate.

Investigating the growth of silicon nanowires on amorphous silicon coated substrates would determine whether silicon nanowire solar cells can be produced in a similar way to amorphous silicon solar cells. That is, by using layers of amorphous silicon and silicon nanowires. This would allow complex structures to be built up. A thin film solar cell generally needs a transparent electrode so that the light can actually get into the semiconductor device. A Transparent Conductive Oxide (TCO) is often used for this purpose. There is very little in the literature about growing silicon nanowires on TCO or amorphous silicon coated substrates. Thus, one of the goals of this work is to produce silicon nanowires on TCO coated glass, uncoated glass and amorphous silicon coated substrates to determine the extent
to which silicon nanowires can be grown on transparent substrates or substrates other than crystalline silicon.

Introducing dopants into bulk crystalline silicon and amorphous silicon changes the electronic characteristics of the material. Introducing dopants into bulk silicon increases the conductance of the material. By using appropriate dopants, p-type and n-type silicon can be produced. These materials can then be used in the production of semiconductor devices such as diodes, transistors and solar cells. Silicon nanowires have previously been doped during growth using both phosphine as an n-type dopant and diborane as a p-type dopant. Silicon nanowires have been doped as either n-type (Wang et al., 2005) or p-type (Pan et al., 2005b). However, other semiconductor nanowires have been doped with two dopants to create homojunctions within the one nanowire or even coated with doped microcrystalline silicon layers to form junctions (Tian et al., 2007). The doping of silicon nanowires is an important step towards creating a solar cell utilising nanowires. Thus, an aim of this project is to determine the feasibility of doping the silicon nanowires produced in the available deposition system using phosphine as an n-type dopant and diborane as a p-type dopant.

The final aim of this project is to produce photovoltaic devices using silicon nanowires in order to incorporate their novel characteristics into the solar cell. It is one of the aims of this project to investigate several device designs in order to produce a thin film silicon nanowire photovoltaic device. These devices would use intrinsic silicon nanowires coated with or embedded in doped amorphous silicon layers. Other devices would use doped silicon nanowires as a p-layer. The electrical characteristics of the nanowire devices created will be investigated using current-voltage measurements. The production of a prototype device that includes silicon nanowires as part of its structure demonstrates that silicon nanowires can be used for thin film photovoltaic applications.

In summary, the aims of this project are as follows:
1) To optimise the growth of silicon nanowires on the existing PECVD / CVD system.

2) To use several different catalysts to find a catalyst that produces high density nanowires at a lower temperature or more cheaply than the usual gold catalyst.

3) To determine if the use of pulsed PECVD improves the growth of silicon nanowires and to what extent doping would be feasible.

4) To find a transparent substrate upon which silicon nanowires will grow and investigate if they can be grown on top of amorphous silicon films, Indium Tin Oxide (ITO) or glass.

5) To determine if the silicon nanowires can be doped in situ using the existing PECVD system.

6) Using the information from the above; the final goal is to produce a silicon nanowire based thin film photovoltaic device.

1.3 Thesis Overview

Structurally this thesis is broken up into several sections. A review of the available literature and general information on the experimental techniques and design is given in the early chapters. The following chapters (5-11) are reports on the various studies undertaken in this project. Several of these reports have been published or presented at conferences and are presented here in an edited or extended form. To provide some links between these sections an overall discussion is given in Chapter 12 followed by the conclusions from the project in Chapter 13.

In more detail, Chapter 2 provides background information and a review of the available literature. This includes sections on the growth of silicon nanowires, common nanowire morphologies and applications. The later part of this chapter gives an overview of amorphous silicon, nano crystalline silicon and their use in photovoltaics.
Chapter 3 details the theory and background information for each of the major experimental systems or techniques used to collect data. The experimental setup and procedure for each of the major experimental systems is detailed in Chapter 4. This chapter also includes a description of the deposition systems used during this work. Specific experimental details for each study are included as part of each chapter.

The details of the base recipe used to grow silicon nanowires are described in Chapter 5. To grow these successfully, several parameters had to be investigated. The affect on the growth of silicon nanowires of temperature, pressure, gas plasma and the catalyst layer thickness is reported in Chapter 5. The optimisation of the basic recipe used in this project for several of the major parameters affecting growth is detailed in Chapter 5. Chapter 6 builds on the recipe and the set of conditions used for silicon nanowire growth in Chapter 5. Chapter 6 describes how the use of Pulsed PECVD affected the growth of silicon nanowires. The use of PPECVD was found to improve silicon nanowire growth.

Using the growth conditions described in Chapters 5 and 6 and following the investigation of the affect of thickness of the catalyst layer in Chapter 5, the effect of using different catalysts could be investigated. The effect of using different catalysts for the production of silicon nanowires via the VLS mechanism is discussed in Chapter 7. Tin and gold were found to be the most productive of the catalysts trialled.

Silicon nanowires were grown on a variety of different materials using the optimised growth conditions developed in Chapter 6. The effect of the substrate on the growth and morphology of the silicon nanowires is explored in Chapter 8. It was found that silicon nanowires were able to be grown on a transparent conducting oxide coated glass substrate.
Further studies were conducted on the deposition parameters when used with the Pulsed PECVD technique discussed in Chapter 6. The parameters that were investigated included the duration of the plasma and silane partial pressures. The samples were produced using the tin and gold catalysts that were highlighted as productive catalysts in Chapter 7. This study was conducted to determine the feasibility of doping the silicon nanowires \textit{in situ} on the existing system. The effect of the various parameters on the nanowire morphology is discussed in Chapter 9.

Electrical contacts to semiconductor thin film devices are often made using aluminium. Silicon nanowire films produced using the Pulsed PECVD as described in Chapter 6 and the productive catalysts found in Chapter 7 were coated with aluminium to determine if the aluminium would stick to the nanowires. In addition to being coated in aluminium, the nanowires films were subjected to damage by a variety of abrasives to test their durability. The morphological changes caused by coating the silicon nanowire film and results of the durability tests are detailed in Chapter 10.

A prototype silicon nanowire based thin film photovoltaic device is demonstrated in Chapter 11. The device was produced using the growth conditions described in Chapter 6. The two productive catalysts from Chapter 7, tin and gold, were used to produce silicon nanowires of different morphologies. As Chapter 8 details, the silicon nanowires could be grown on transparent conducting oxide coated glass, allowing light to get to the photovoltaic device. The electrical properties of the silicon nanowires were investigated in their undoped states. Several device designs using combinations of doped and intrinsic silicon nanowires and amorphous silicon were trialled. The details of the devices, their design, implementation and characteristics are discussed in Chapter 11.
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The overall results of this project are brought together and discussed in Chapter 12. Conclusions drawn from the discussions and the overall outcomes of this project are detailed in Chapter 13.
2.1 Silicon

Silicon is one of the most abundant elements in the Earth’s crust (25.7%) second only to oxygen (Lide, 2005). Silicon is usually found in the form of oxides and silicates, such as sand and quartz. Arguably one of the more important and versatile elements, silicon can be used to produce everything from bricks to computer chips. Berzelius is generally credited with the discovery of silicon in its amorphous form in 1824. Crystalline silicon was created by Deville in 1854. Recently a supply shortage has driven up the price of solar grade silicon from $9/kg (USD) in 2000 to $200/kg (USD) in 2006 (Purvis, 2006). Takashi Tomita, Head of Sharp Solar (a solar cell manufacturer), Japan, has stated ‘a shortage of polysilicon materials would lead to an increase in prices of polysilicon and could ultimately lead to a stagnation of the solar cell market’ (Purvis, 2006). Alternatively to stagnation of the market, a shortage of solar grade silicon could lead to the development or increased demand for thin film solar cells due to the smaller quantities of material required to produce them.

2.1.1 Crystalline Silicon

Crystalline silicon (c-Si) forms the basis of many of today’s integrated circuits as it is a readily available semiconductor which is relatively easy to process and dope to form semiconductor devices. Crystalline silicon has a type of face centred cubic structure and is dark grey in colour with a slight bluish tinge. When cleaned and etched or polished, crystalline silicon is highly reflective. A photo of a sample of crystalline silicon is shown in Figure 2-1. Devices made from crystalline silicon include many integrated circuits, diodes and solar cells. High purity crystalline silicon is typically produced using the Czochralski process (Lide, 2005). Crystalline silicon was the material used in the earliest photovoltaic devices, or solar cells, and is still commonly used for this purpose due to the high efficiency of the resulting devices.
Silicon crystals are typically cut to produce wafers with different surface orientations such as (111), (100) and (110). The nomenclature \((xyz)\) refers to the orientation of the crystal plane defined in terms of the axes \((a_1, a_2, a_3)\). This is illustrated in Figure 2-2 which shows a unit cell of the face-centred-cubic crystal structure with the different crystal planes. The nomenclature \([xyz]\) refers to a direction as described by a vector where \(x, y\) and \(z\) are the components of the vector in terms of the axes \((a_1, a_2, a_3)\). An example \([111]\) vector is shown in Figure 2-2. Figure 2-2 also shows the arrangement of the atoms in a face-centred-cubic unit cell, the basic unit of a crystal lattice. Silicon itself has a face-centred diamond cubic crystal structure with a space group of \(Fd3m\).
2.1.2 Amorphous Silicon

Amorphous silicon (a-Si) is a glass-like material that structurally does not have long range structural order and is randomly oriented. Due to the random orientation of the material, the absorption coefficient of light in amorphous silicon tends to be higher than that of crystalline silicon. This allows thin film devices to be fabricated from amorphous silicon that can absorb similar quantities of light to much thicker crystalline silicon slices. Because of this, the fabrication of thin film devices is one of the main uses of amorphous silicon. In addition it is a relatively straightforward process to create doped layers of amorphous silicon. The dopant layers can be produced by introducing dopant gasses during the deposition of amorphous silicon.

Amorphous silicon can be produced using a variety of deposition methods. These methods include a) physical deposition methods such as sputtering and b) chemical vapour deposition.
techniques such as Plasma Enhanced Chemical Vapour Deposition (PECVD) and Hot Wire Chemical Vapour Deposition (HWCVD).

One of the main uses of amorphous silicon is in the solar cell industry for the fabrication of cheap thin film solar cells. Amorphous materials are glass-like, randomly structured materials which gives amorphous solar cells some fairly unique properties and problems. An illustration of this glass like structure, hydrogenated amorphous silicon, is shown in Figure 2-3. Amorphous silicon by itself has many dangling bonds which trap charge carriers thereby reducing the efficiency of the cell. By creating hydrogenated amorphous silicon (a-Si:H), a hydrogen and silicon alloy, many of the traps can be eliminated (Wilson, 1980). This allows it to be used in photovoltaic applications with useful efficiencies. In Figure 2-3 the dangling bonds have hydrogen atoms attached so as to passivate them and eliminate the traps.

![Figure 2-3: Representation of the structure of hydrogenated amorphous silicon.](image)
Different thicknesses of amorphous silicon films have different colours. Amorphous silicon has a distinctive red-orange colour when produced as a thin film of approximately 500nm in thickness on glass. This can be seen in Figure 2-4. Thinner (~200nm) films tend to have a yellow colouration. Due to the variations in the thickness of the thin film shown in Figure 2-4 below, although not obvious, interference fringes can be seen around the edge of the glass slide.

![Figure 2-4: Photograph of amorphous silicon on glass (~500nm).](image)

### 2.1.3 Polycrystalline Silicon

Polycrystalline Silicon is a variant of silicon that consists of a series of small crystallites that have grown together with an extremely high crystallinity or proportion of crystalline material. Typically, polycrystalline silicon is defined as having a grain size (crystallite diameter) of between 10 and 30µm and a crystalline fraction of close to 100% (Cabarrocas, 2004). Polycrystalline material is usually deposited by chemical vapour deposition (Cabarrocas, 2004) or hot wire chemical vapour deposition (Lee et al., 2002). Polycrystalline silicon can be doped and used to fabricate solar cells, amongst other devices.
A variant of polycrystalline silicon, polymorphous silicon, structurally consists of nanocrystallites dispersed in a relaxed a-Si:H network matrix (Roca i Cabarrocas et al., 2002).

2.1.4 Microcrystalline Silicon

Microcrystalline silicon (µc-Si) is structurally formed of a series of micron-sized crystallites embedded in an amorphous silicon matrix, consisting of crystalline, amorphous phases and grain boundaries (Droz et al., 2003). Microcrystalline silicon is commonly defined as having a grain size between 10 and 20nm and a crystalline fraction of between 10 and 100% (Cabarrocas, 2004). Microcrystalline silicon is an attractive material for electronic device applications due to its high carrier mobility and hence, high electrical conductivity (Das and Jana, 2004). Microcrystalline silicon can be produced by PECVD (Fontcuberta i Morral and Roca i Cabarrocas, 2001), Hot Wire Chemical Vapour Deposition (HWCVD) (Carius et al., 2003) and Very High Frequency PECVD (VHF-PECVD). The crystallinity of the material is known to vary with the deposition conditions (Droz et al., 2003). This variant of silicon is also commonly used in the photovoltaic industry to produce single junction and micromorph tandem solar cells (Meier et al., 2004a).

2.1.5 Nanocrystalline Silicon

Nanocrystalline silicon (nc-Si) is similar to microcrystalline silicon as it consists of crystallites embedded in an amorphous silicon matrix. Nanocrystalline silicon is commonly defined as having a grain size between 2 and 5nm and a crystalline fraction of between 10 and 80% (Cabarrocas, 2004). In addition to the amorphous and crystalline phases, an amorphous buffer layer, that can be crystallised by post-growth annealing, is also present in nanocrystalline silicon (Gourbilleau et al., 1999). Nanocrystalline silicon can be produced using Radio Frequency (RF) sputtering (Gourbilleau et al., 1999), CVD (Zhang and Han, 2002) and PECVD (Wang et al., 1992). This form of silicon is an interesting material as it has
good optical and electronic properties. It can be used to produce solar cells (Yue et al., 2006) and electroluminescent devices (Sato et al., 2003).

2.1.6 Nanostructured Silicon
Silicon materials consisting of highly textured structures of nanometre scale are known as nanostructured silicon. These structures can be free standing rather than being embedded in a substrate. Nanostructured silicon is of much interest as the properties of this material differ from bulk silicon, allowing novel applications.

2.1.6.1 Quantum Wires / Nanowires
There has been much recent interest in silicon-based quantum wires (or nanowires). Crystalline silicon nanowires are a new form of semiconductor material, the properties of which differ from those of bulk silicon. A nanowire is a quasi one-dimensional structure that has a nanoscale diameter, a length often in the micron range and a high aspect ratio. The aspect ratio refers to the ratio of the diameter to the length. Nanowires have diameters ranging between a few nanometres to the low hundreds of nanometres and lengths ranging up to a few millimetres. A nanowire usually has an approximately circular cross section. Nanowires can be bonded to, or embedded in, the surface of a substrate throughout their entire length. Or they can be freestanding, being attached to a substrate by only one end. Nanowires can also be produced in a bulk form where they are not attached to a substrate at all.

Silicon based nanowires, that is, nanowires that are composed at least partially of silicon, include SiC nanowires (Wieligor et al., 2005), SiO\textsubscript{x} (Dikin et al., 2003, Noda et al., 2005) and nanowires consisting purely of silicon (Westwater et al., 1997).
A SiO$_x$ nanowire consists in its entirety of silicon oxide (Dikin et al., 2003, Noda et al., 2005). This is a necessary distinction as many purely silicon nanowires are coated in an amorphous silicon oxide sheath, due to oxidation of the nanowires after their growth yet maintain a crystalline silicon core.

A silicon nanowire is composed of silicon in either an amorphous phase or a crystalline phase. The amorphous phase nanowires tend to exhibit worm-like structures that curve and change direction gradually (Hofmann et al., 2003) while the crystalline phase is generally straight and tends to exhibit growth defects such as kinking. These growth defects, known as kinks, are abrupt changes in growth direction. Examples of both the crystalline and amorphous morphologies can be seen in Figure 2-5. Crystalline silicon nanowires are composed of an elongated single crystal of silicon of very small diameter. The nanowire is often sheathed in an oxide layer due to oxidation after the growth of the nanowire. The nanowire itself can be left intrinsic (undoped) or doped to be either n-type or p-type. A combination of dopants can be used to create semiconductor junctions and devices within the one nanowire.

Silicon nanowires are often produced with a tapered morphology. That is, the diameter of the nanowire narrows from the base towards the tip. These tapered wires range from needle like-structures to cone shaped structures known as silicon nanocones (Shirai et al., 2005). Silicon nanowires can be fabricated using a range of different techniques and growth mechanisms, allowing diverse potential applications. Some common nomenclature that is used when describing silicon nanowires is shown in Figure 2-5.
2.2 The Presence of the Term ‘Silicon Nanowires’ in the Literature

Many papers in the literature dealing with silicon nanowires and other semiconductor nanostructures begin with an introductory sentence similar to: ‘Lately there has been a great deal of interest in silicon nanowires, silicon nanostructures and nanoscale semiconductors’. There are a number of variations but all express the same sentiment that a) there has been an increase in interest in silicon nanowires and b) that there is a large amount of recent interest.

To verify these two comments, a search was run through a series of journal databases for where the terms ‘silicon’ and ‘nanowire’ appeared together within the one paper, for each year. Although not all of the papers this search retrieved dealt specifically with silicon nanowires the level of interest in the subject was determined from this search. Because large silicon nanowires have been referred to as ‘silicon filaments’ or ‘filamentary crystals’ as far back as 1964 by Wagner and Ellis (Wagner et al., 1964), not all articles dealing with silicon
‘nanowires’ were retrieved. Because each database tends to list different journals, three separate journal databases were used. These were:

- SCOPUS (Elsevier).
- Science Direct.
- Inspec (IET).

Three databases were used to see if the trend was consistent across a variety of journal subsets.

According to the databases, the words ‘silicon’ and ‘nanowire’ first appeared together in the one paper in 1993. So, a search was conducted through all three databases for journal articles appearing in each year from 1993 to 2007 with the relevant search terms. The results are displayed in Figure 2-6.
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Figure 2-6: Silicon nanowire publications in three journal databases (1993-2005).

From Figure 2-6 three things can immediately be observed:

1) There has been an increase in the number of publications relating to silicon nanowires since 1993.

2) The number of publications in 2005 exceeds those in any previous years.

3) The databases have different number of relevant papers. Hence, it is important to choose a journal database that deals with the subject a researcher is investigating so as to retrieve the largest number of articles. Or, more accurately, use more than one database.
These observations support the sentiment expressed in the introductory few lines of this section, that the number of papers dealing with silicon nanowires is increasing and that there has been a great deal of recent interest in silicon nanowires.

From Figure 2-6 it can be seen that the number of journal publications relating to silicon nanowires had increased almost exponentially from 1993 to 2005 in all three journal databases. From 2005 this rapid increase has started to taper off. This may indicate that the number of new research groups interested in silicon nanowires has plateaued. The groups that have an interest in and are able to produce silicon nanowires had probably already started researching and publishing papers by 2005.

The countries that are producing the bulk of the silicon nanowire related papers can be gleaned from examination of the journal databases. The origin of the papers can be determined by searching for ‘silicon’, ‘nanowire’ and the name of a country. Some 85% of all papers published since 1993 relating to silicon nanowires originate in ten countries. Figure 2-7, shows the distribution of the number of papers for each of the top ten countries for the years 1993 to 2006. The data for this chart was sourced from the Inspec journal database.
Figure 2-7: Nanowire publication broken down by year and country from the Inspec database for the years 1993 - 2006.

On examination of the data from the database search, it can be seen that the most prolific countries in terms of total publications on Si nanowires are the United States, China and Japan. There are 32 countries in which researchers have published papers relating to silicon nanowires with most producing a few papers in the years to 2006. Figure 2-7 illustrates which portion of the total number of nanowire publications has been published by which country.

A few more observations can be made. There is a global increase in interest, evidenced by the number of publications, in silicon nanowires. Some countries, such as China and the United States, are publishing an increasing number of journal papers. Other countries, such as Japan, are not showing the same increase number of publications but are showing a more steady level of publication.
In summary, it has been shown that there has been an exponential increase in the number of publications relating to silicon nanowires since 1993. This agrees with the often expressed sentiment that there has been an increase in the level of interest in silicon nanowires and that there has been a high level of interest in recent years. After the almost exponential growth in publications up to 2005, the growth rate has started to taper off. The top ten silicon nanowire producing countries, in terms of publications, have been identified and are shown in Figure 2-7. Some of these countries were publishing an increasing number of papers while others were almost constant.

2.3 Growth Mechanisms
Many different growth mechanisms have been used to grow silicon nanowires. Each growth mechanism has its own defining characteristics and is often coupled with a specific deposition technique to create silicon nanowires.

2.3.1 The Vapour Liquid Solid (VLS) Mechanism
The most commonly used mechanism invoked to describe the growth of silicon nanowires is the Vapour Liquid Solid (VLS) mechanism. This was first proposed by Wagner and Ellis in 1964 to describe the growth of silicon filaments (Wagner and Ellis, 1964). The VLS mechanism uses a vapour phase reactant (\(\text{SiI}_2\) or \(\text{SiH}_4\)), a liquid catalyst and a solid substrate to produce small diameter filaments or crystals of silicon (Wagner and Ellis, 1964). The silicon comes from the disproportionation of \(\text{SiI}_2\) or the hydrogen reduction of \(\text{SiH}_4\). The VLS mechanism can be used to produce silicon nanowires.

The VLS mechanism uses a liquid catalyst that absorbs material from the surrounding vapour, often \(\text{SiI}_2\) or \(\text{SiH}_4\). Thin films of metallic catalysts are often used to grow silicon nanowires. A thin layer of metal catalyst is deposited onto a substrate under vacuum and is then placed in a deposition chamber which is also under vacuum. The substrate is heated
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until the metal catalyst melts. In the case of gold on a silicon substrate, a eutectic with silicon forms at 363°C. The liquid catalyst forms small droplets, or islands, on the surface of the substrate. The size of the island determines the size of the resulting nanowire. The gas source of silicon is then introduced and is thermally decomposed and absorbed by the liquid metal. When the catalyst becomes supersaturated with silicon, crystalline silicon is deposited underneath the metal droplet. As material is deposited, the liquid catalyst droplet rides on top of the growing nanowire or crystal filament (McIlroy et al., 2004). The presence of a metal catalyst on the end of a nanowire is indicative of the VLS mechanism (Wagner and Ellis, 1964).

The catalyst plays an important role in the growth of nanowires or filaments via the VLS mechanism. The choice of catalyst depends on the type of nanowire that is to be produced as the material to be used must be soluble in the catalyst (McIlroy et al., 2004). It is also desirable that the catalyst produces a liquid alloy or eutectic droplet with a relatively low melting point (Wagner and Ellis, 1964). A liquid catalyst droplet acts as a preferred site for the deposition of material from the vapour phase reactants (Wagner and Ellis, 1964). To lower the melting point of the catalyst further, droplets or clusters with small diameters can be used as it is known that the melting point of droplets with a diameter below 200nm is lower than that of the bulk material (McIlroy et al., 2004). In the case of lead, for example, the melting point is decreased by about 200K for particles of a radius of 3nm (Coombes, 1972). So where the catalyst particle size is below 200nm, the eutectic point of the nanoparticles and silicon will be reduced, allowing for lower temperature growth of silicon nanowires via the VLS mechanism. It has previously been shown by Westwater and co-workers (1998) that silicon nanowires can be grown via thermal CVD at temperatures as low as 320°C using gold as a catalyst which is well below the eutectic point of gold and silicon.
The morphology of the nanowire is also determined in part by the catalyst. The diameter of the catalyst droplet determines the size of the resulting nanowire. It has been shown using Au nanoclusters, which are nanoparticles of Au, that the diameter of the grown nanowires increases proportionally with cluster diameter (Cui et al., 2001). It was also found that the nanowire diameter was slightly larger than the cluster diameter which was explained as being consistent with the formation of an Au/Si alloy droplet (Cui et al., 2001). The diameter of the nanowire can be smaller or the same size as the diameter of the droplet from which it grew, but never larger (McIlroy et al., 2004).

Nanowires or small diameter silicon crystals, known as silicon whiskers, produced via the VLS mechanism have some distinct characteristics. Silicon whiskers grown via this mechanism do not contain an axial screw dislocation and a small droplet is usually present at the end of the silicon whisker or nanowire during growth (Wagner and Ellis, 1964). Crystalline silicon nanowires or whiskers grown via the VLS mechanism tend to grow in the [111] direction (Wagner and Ellis, 1964). This allows the direction of growth relative to the substrate to be controlled by judicious selection of the substrate. A silicon nanowire grown via the VLS mechanism on a (111) crystalline silicon substrate will grow perpendicular to the substrate (Wu et al., 2002).

The VLS mechanism is used with a variety of deposition techniques. These include flow reactors (Dikin et al., 2003), chemical vapour deposition (Westwater et al., 1998) and plasma enhanced chemical vapour deposition (Hofmann et al., 2003, Westwater et al., 1997).

2.3.2 The Solid Liquid Solid (SLS) Mechanism

Another growth mechanism that uses a metal catalyst to assist in the growth of silicon nanowires is the Solid Liquid Solid (SLS) mechanism as proposed by Yan, Xing and co-workers (2000). They used the SLS mechanism for the growth of amorphous silicon
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nanowires with a nickel catalyst. This SLS mechanism is analogous to the VLS mechanism described above with a key difference. This difference is the use of a solid phase source of silicon rather than a vapour phase source. Yan, Xing and co-workers have also shown that the SLS mechanism can be used to produce silicon nanowires using a gold catalyst (Xing et al., 2003). The technique this group used to produce nanowires involved heating a gold coated silicon (c-Si(111)) substrate in a quartz-tube furnace under a flowing H₂ atmosphere at 200 torr for one hour. The SLS mechanism has three phases. Firstly Au-Si droplets form on the substrate when the substrate temperature is raised to the growth temperature. This forms a solid-liquid interface between the silicon substrate and the liquid catalyst droplet. In the second phase, the H₂ flowing over the surface of the droplets collides with and exchanges energy with the Si atoms on the surface of the droplets. The continual collision of the H₂ with the droplets induces supersaturation at the surface of the droplets. Silicon atoms then precipitate out to nucleate the nanowires, forming a second solid-liquid interface between the liquid droplet and the nucleated nanowire. The third and final phase of the SLS mechanism is the axial growth of the silicon nanowire. The compositional gradient between the two solid-liquid interfaces maintains the diffusion of Si atoms from the substrate to the growing nanowire, via the liquid catalyst droplet, allowing the growth of the silicon nanowire to continue (Xing et al., 2003).

Pan, Lim and co-workers (2005) have used similar growth techniques to grow silicon nanowires. They also proposed a solid liquid solid mechanism as being partially responsible for the growth of their silicon nanowires (Pan et al., 2005a).

2.3.3 Oxide Assisted Growth (OAG)

A number of different groups have identified that oxides contribute to the growth of silicon nanowires. Pan, Lim and co-workers (2005) have proposed that the silicon nanowires they have produced by thermal evaporation have been grown using an oxygen-assisted growth mechanism. The source of the oxygen is either the substrate or trace impurities in the He
which flowed through their furnace. The oxygen forms SiO$_x$ with the evaporated silicon; the SiO$_x$ then acts as seeds for the growth of silicon nanowires (Pan et al., 2005).

Shao and co-workers (2005) have grown silicon nanowires by thermal evaporation of SiO powder which was heated to 1250°C in a tube furnace. A carrier gas of 95% argon and 5% hydrogen was used during fabrication (Shao et al., 2005). The growth of these nanowires was also attributed to an oxide assisted growth mechanism.

### 2.3.4 Sulphide Assisted Growth (SAG)

Niu, Sha and Yang (2004) have proposed a Sulphide Assisted Growth (SAG) mechanism for the growth of silicon nanowires. They found that nanowires could be grown when sulphur powder was used as a catalyst in a low-vacuum CVD system. The sulphur was found to aid in the growth of silicon nanowires. Niu, Sha and Yang (2004) proposed that the growth process occurs in two steps. Firstly sulphur reacts with a silicon substrate to produce SiS at a temperature of ~900°C. The second step occurs at a higher temperature of ~1000°C where SiS decomposes to Si and SiS$_2$ (Niu et al., 2004b). Silicon nanowires grew from the Si generated by the second step. The SiS compound acts as a nucleation site for the growth of silicon nanowires and remains at the tip of the nanowire during their growth. This sulphide assisted growth mechanism is also known as silicon compound assisted growth and is similar to oxide assisted growth.

### 2.3.5 Stress Driven Growth

An alternate nanowire growth mechanism to those previously mentioned involves the growth of silicon nanowires by a stress driven growth mechanism as proposed by Prokes and Arnold (2005). They found that silicon nanowires could be grown on a silicon substrate in a furnace without the presence of a silicon vapour or a metal catalyst. They found that wire growth would only occur if a native oxide layer was present on the silicon substrates and only after
crack formation at the high temperatures used, as the nanowires were found to nucleate from the cracked regions. The different thermal expansion coefficients of SiO\textsubscript{x} and crystalline silicon led to the creation of the cracks and a stress gradient in the sample. Prokes and Arnold (2005) proposed that this leads to the transport of silicon atoms from the stressed regions to the stress free regions resulting in the nucleation of nanowires out of the cracks. They also found that this growth would not occur without the presence of flowing hydrogen gas in the furnace. Prokes and Arnold (2005) proposed that the diffusion kinetics of the silicon is enhanced by the presence of hydrogen.

2.3.6 Other Growth Mechanisms
A growth mechanism described by Kamins and co-workers (2000) used a solid phase particle of titanium and a vapour containing silicon, such as SiH\textsubscript{4}, to create silicon nanowires by a CVD process. This mechanism can be termed the Vapour Solid (VS) growth mechanism. In this growth mechanism solid titanium containing islands are created using CVD and TiCl\textsubscript{4} in argon as a gas precursor on a silicon substrate. These islands are exposed to the vapour containing silicon at temperatures between 640°C and 670°C and nanowires are grown. This growth temperature is far below the eutectic point of silicon and titanium (~1300°C) which indicates that the growth process is not the VLS mechanism. Kamins and co-workers (2000) found that the nanowire was grown by a titanium catalysed decomposition of Si gas with the nanowire grown by extrusion from the base where the solid particle remains. A characteristic of this growth mechanism is the existence of a solid titanium containing particle at the base of the nanowire (Kamins et al., 2001) as opposed to the VLS mechanism where it is at the tip.

A gallium catalysed growth mechanism has been used by other groups to produce Si nanowires and SiO\textsubscript{x} nanowires. Hu, Liu and Wang (2003) produced highly aligned SiO\textsubscript{x} nanowires using millimetre sized gallium droplets without a gas source of silicon. They placed gallium droplets on Si wafers which were heated to 900–950°C in the presence of O\textsubscript{2} and
argen. They found that one droplet of gallium creates thousands of nanowires and that these nanowires did not have a catalyst particle present at their tips. Hu and co-workers (2005) observed that a pit was etched into the silicon substrate by the hot gallium droplet providing a source of silicon for the growth of nanowires. Hu, Liu and Wang (2003) proposed a growth mechanism with the following steps.

1) The silicon wafer was etched by the hot gallium droplets.

2) Some Si atoms were dissolved into the gallium and acted as a source of silicon for the growth of the silicon oxide nanowires.

3) The gallium droplet absorbed oxygen from the surrounding atmosphere.

4) SiO$_x$ formed and precipitated out as it is insoluble in gallium, thus forming nanowires.

Sharma and Sunkara (2004) have used droplets of gallium and silane plasma on a non silicon substrate to produce silicon nanowires. The nanowires they produced did not have any gallium or other catalyst present at their tips which suggests a base growth mechanism similar to that used by Hu, Liu and Wang (2003). The mechanism proposed by Sharma and Sunkara (2004) has the following steps.

1) Silyl radicals (SiH$_3$) were adsorbed onto the surface of the molten gallium droplet by atomic hydrogen mediation.

2) The migration and diffusion of Si-Ga complexes into the bulk molten material.

3) The nucleation of the silicon nanowires followed by surface segregation of the nuclei.

4) The nuclei then grew in one dimension based upon basal attachment kinetics (Sharma and Sunkara, 2004).
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2.4 Growth Techniques

Silicon nanowires have been grown using a number of methods and deposition techniques. Each deposition technique has its own set of advantages and disadvantages. From the variety of growth techniques used it can be seen that silicon nanowires can be grown without the need for application-specific equipment. Alternatively, existing apparatus can be adapted to the purpose. The reason for the wide variety of growth techniques used to produce silicon nanowires would be the adaptation of existing deposition techniques and equipment for this purpose.

2.4.1 Thermal Evaporation / Furnace Style

Thermal evaporation using a furnace is a frequently used method of fabricating a variety of nanomaterials including carbon nanotubes and silicon nanowires either on substrates or in bulk. Thermal evaporation is a method whereby a solid source of silicon is placed in a quartz or alumina tube which is loaded inside a furnace. The solid source of silicon can be:

- Silicon powder, with a powdered catalyst which has been hot pressed into a plate (Yu et al., 1998a).
- Silicon powder without a catalyst (Noda et al., 2005).
- Silicon oxide, for the oxide assisted growth process (Shao et al., 2005).
- A single crystal of silicon (Chueh et al., 2005).

The quartz or alumina tube can be kept at a specific pressure of up to 100 torr of argon (Yu et al., 1998a). Alternatively a gas or mixture of gases such as 10% hydrogen in helium (Byon et al., 2005), hydrogen (Xing et al., 2003) or argon and hydrogen (Prokes and Arnold, 2005) can be passed through the furnace or tube at flow rates of between 50 sccm (Byon et al., 2005) and 80 sccm (Xing et al., 2003). The furnace can be heated to temperatures of between 900°C (Hu et al., 2003) and 1350°C (Shi et al., 2005). Growth times range from 30 minutes...
Some research groups use a catalyst to encourage the growth of silicon nanowires. The catalysts used include Fe (Yu et al., 1998a, Chueh et al., 2005), Ga (Hu et al., 2003) and Au (Xing et al., 2003).

The silicon nanowires are grown either in bulk, appearing as a yellow sponge like product on the tube itself (Yu et al., 1998a, Shi et al., 2005) or on a silicon substrate also placed in the tube (Byon et al., 2005, Shao et al., 2005, Prokes and Arnold, 2005).

Thermal evaporation is a technique which fabricates silicon nanowires in a relatively straightforward manner either in a bulk form or on silicon substrates. In most situations the high furnace temperatures evaporate the silicon and it forms nanowires via the VLS mechanism. Some nanowires however, grow by other mechanisms such as the oxide assisted growth mechanism (Shao et al., 2005).

2.4.2 Laser Ablation

Laser ablation is similar to thermal evaporation as it involves a solid phase of silicon and a source of energy to evaporate, or in this case ablate, the silicon to allow nanowire formation to occur. Laser ablation is not as popular a method of fabricating nanowires as thermal evaporation, with only a few research groups using this technique.

Laser ablation involves using a laser to ablate a target containing silicon, plus in some cases, a catalyst and doping materials. The target can consist of silicon monoxide and boron oxide when used to create boron-doped silicon nanowires by laser ablation at high temperatures (Ma et al., 2001). Yu et al. (1998) used a target formed of pressed silicon powder, silica powder and powdered Fe as a catalyst. Catalytic laser ablation was also used by Fukata et al. (2005) with a target consisting of silicon and a nickel catalyst. The targets and substrates were placed in quartz tubes which were heated in a furnace to temperatures between 1000°C and 1200°C.
Once the required temperature was reached, a laser was focused on the target (Yu et al., 1998b). The laser used for ablation can be scanned across the target to avoid continuous irradiation of one portion of the sample (Fukata et al., 2005b). The use of different ambient gasses can alter the diameter of silicon nanowires grown by excimer laser ablation with Ar (5% in H₂) producing smaller diameter wires than He (Zhang et al., 1999).

### 2.4.3 Gas Source Molecular Beam Epitaxy (MBE)
Gas Source Molecular Beam Epitaxy (MBE) has been used by several research groups to produce silicon nanowires. Ishida and co-workers (2003) produced silicon nanowires on a Si(111) substrate using a gold catalyst and Si₂H₆ as a gas source for MBE at 650°C. Liu and co-workers (1999) produced silicon nanowires using MBE on a variety of different substrate orientations all coated with a gold catalyst. The silicon was deposited by MBE with a Si₂H₆ pressure of 1×10⁻⁷ torr and at a temperature of 700°C. Gas source MBE is a versatile technique but requires some specialised equipment.

### 2.4.4 Chemical Vapour Deposition (CVD)
Chemical Vapour Deposition (CVD) is currently the most widely used method to grow silicon nanowires. It is a versatile technique that can produce a range of materials from semiconductors to diamonds. CVD uses vapour phase chemical precursors which are reacted or decomposed onto the substrate to produce the desired material. CVD, for the growth of silicon nanowires, is used with a wide range of parameters, with or without a catalyst. However, the procedure is similar throughout the different variations. Crystalline silicon is often used as a substrate on which to grow the silicon nanowires (Westwater et al., 1997). A catalyst such as gold (Westwater et al., 1997, Cui et al., 2001), titanium (Kamins et al., 2000) or zinc (Yu et al., 2000) is deposited onto the substrate. The substrate is then heated in the presence of a silicon containing gas such as silane (SiH₄) (Westwater et al., 1998, Kikkawa et al., 2005, Cui et al., 2001), disilane (Huo et al., 2004), SiH₂Cl₂ or SiCl₄, at pressures ranging
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from $10^{-8}$ torr (Ross et al., 2005) to 735 torr (Kikkawa et al., 2005). Silicon nanowires have also been grown using atmospheric pressure chemical vapour deposition (Kulkarni et al., 2005). The silicon containing gas is often diluted with hydrogen (Niu et al., 2004a, Kulkarni et al., 2005) or argon (Kikkawa et al., 2005). The substrate is heated to temperatures between 320°C (Westwater et al., 1998) and 950°C (Kulkarni et al., 2005). The most common substrate used is crystalline silicon (Yu et al., 2000) of varying orientations. However glass substrates coated with indium tin oxide (ITO) and aluminium oxide/titanium oxide (ATO) have also been used (Huo et al., 2004).

From the number of variations on the technique and range of parameters used, chemical vapour deposition is clearly a very versatile technique. Due to its versatility CVD is one of the more widely used techniques as demonstrated by the number of groups using this technique to grow silicon nanowires.

2.4.5 Plasma Enhanced Chemical Vapour Deposition (PECVD)

Plasma Enhanced Chemical Vapour Deposition (PECVD) is a variant of chemical vapour deposition which is widely used in the production of amorphous or microcrystalline silicon for thin-film devices. It has also been used by some research groups to fabricate silicon nanowires. PECVD that often uses a 13.56MHz radio frequency (RF) (Hofmann et al., 2003) or a microwave signal (Sharma and Sunkara, 2004) to crack or decompose the precursor gasses. In conjunction with a metal catalyst, PECVD can be used to produce silicon nanowires. For growing silicon nanowires, PECVD is often conducted using silicon substrates with gold catalyst layers (Hofmann et al., 2003). Alternatively gallium droplets on alumina, quartz and pyrolytic boron nitride substrates have been used (Sharma and Sunkara, 2004). Silicon nanowires are often produced with a precursor gas of silane.
Typical conditions for the growth of silicon nanowires by RF PECVD consist of a substrate
temperature of 380°C and a chamber pressure of between 0.3 torr and 1.8 torr (Hofmann et
al., 2003). Typically the growth time is in the order of between 15 minutes and 90 minutes
(Hofmann et al., 2003).

Sunkara and co-workers (2001) have used a microwave plasma reactor to grow silicon
nanowires. In their work a silicon substrate coated in gallium was exposed to a 700W
microwave plasma of 1:100 H$_2$ in N$_2$. The substrate temperature was measured by an infrared
pyrometer to be about 400°C. In this technique the hydrogen plasma etched areas of the
silicon substrate to produce silyl radicals in a vapour phase (Sunkara et al., 2001). Typical
conditions for the growth of silicon nanowires using a microwave frequency plasma consist
of a 2% SiH$_4$/H$_2$ gas mixture at a total pressure of 40 torr and a plasma power of 700W
(Sharma and Sunkara, 2004). The substrate was kept at a temperature of 550°C and the
deposition time varied between 1 and 6 hours (Sharma and Sunkara, 2004). Sunkara and co-
workers (2001) found that the length of the nanowires grown via this technique was
proportional to the duration of the experiment which ranged from 1 to 9 hours.

PECVD is a useful technique for producing silicon nanowires as it is known to significantly
increase the nanowire growth rate (Hofmann et al., 2003). Although amorphous silicon is also
deposited on to the substrate, the metal droplets preferentially encourage the growth of the
crystalline nanowires. PECVD is a relatively simple variant of the commonly used CVD
technique.

### 2.4.6 Pulsed Plasma Enhanced Chemical Vapour Deposition (PPECVD)

A further modification of the PECVD technique is known as Pulsed PECVD (PPECVD).
This involves the modulation of the 13.56MHz RF signal used to generate the plasma
(Morrison et al., 2002). Use of suitable apparatus allows the modification of the modulation
frequency as well as the ratio of plasma on-time to off-time (mark space ratio). For the
deposition of microcrystalline silicon thin films a modulation frequency of between 1kHz
and 100kHz and a mark space ratio of 10% to 50% is used (Morrison et al., 2003). This
technique increases the deposition rate of a-Si, nc-Si and µc-Si while suppressing the dust
formation that tends to occur when the deposition rate is increased simply by increasing the
plasma power (Das et al., 2003). It follows that Pulsed PECVD may increase the deposition
rate of silicon nanowires. The application of this technique to the production of silicon
nanowires in this thesis is detailed in Chapter 6.

2.4.7 Other Deposition Techniques

A deposition method used by Marsen and Sattler (1999) involved the growth of silicon
nanowires from atomic vapour in Ultra High Vacuum (UHV). The silicon was deposited by
room temperature magnetron sputtering under an 8 mtorr argon pressure (Marsen and
Sattler, 1999).

The substrate used was highly oriented pyrolytic graphite. This deposition technique
produced bundles of 20-30 nanowires with lengths greater than 100nm and diameters from 3
to 7nm (Marsen and Sattler, 1999).

2.4.8 Summary

The use of many and varied growth techniques evidence a wide range of deposition
techniques and growth conditions. Two of the more important growth parameters when
producing silicon nanowires are the substrate temperature and ambient pressure of a vapour
phase of silicon or simply a carrier gas. The chart on the next page (Figure 2-8) illustrates the
variety of growth regimes that have been used. Most nanowires are produced at a pressure
range of between $10^{-2}$ torr and $10^{3}$ torr with temperatures above 350°C and below 800°C.
These growth conditions can be readily attained using a variety of deposition techniques and
show that extreme conditions, such as very high temperature, are not necessary for nanowire growth.

![Figure 2-8: Silicon nanowire growth regimes.](image)

2.5 Nanowire Properties

Silicon nanowires have unique properties, many of which are changed by the morphology of the nanowire. The morphology of the nanowire includes the diameter, length, crystallinity, growth orientation and the presence of any features such as a catalyst tip. The morphology of the nanowire can also affect properties such as the band-gap and electrical characteristics. These properties of silicon nanowires, and other nanostructures, tend to differ from that of bulk silicon.
2.5.1 Morphology

The morphology of silicon nanowires is dependant on how they are grown and what growth mechanism is used. Nanowires grown via the VLS mechanism have a characteristic catalyst particle left at the tip of the nanowire after growth (Wagner and Ellis, 1964) whereas other growth mechanisms do not. Crystalline nanowires tend to exhibit growth defects such as kinking.

There are a number of parameters that are known to affect the morphology of silicon nanowires. Aspects of the morphology that are readily identifiable are the diameters of the nanowires, the number of kinks (growth defects) present in the nanowires and the density of nanowire growth. Westwater and co-workers (1998) have shown that silicon nanowires tend to exhibit kinking under higher pressures (>3.0 torr) and / or lower temperatures (<440°C) using CVD growth. These silicon nanowires tend to spontaneously change growth direction during growth (Westwater et al., 1998).

Silicon nanowires often consist of a crystalline silicon core surrounded by an amorphous silicon oxide sheath of varying thickness. An example of this is the nanowires grown by low vacuum CVD (Niu et al., 2004b). Nanowires grown using molten gallium as a catalyst also exhibit a crystalline core with an amorphous oxide layer (Sharma and Sunkara, 2004).

The growth direction of silicon nanowires is a characteristic of morphology that is often affected by the growth mechanism and the growth technique used. Nanowires grown using molten gallium as a catalyst tend to grow along the [100] direction (Sharma and Sunkara, 2004). In comparison, by using a VLS mechanism with silane as a vapour phase source of silicon, and gold as a catalyst, nanowires were produced which tended to grow in the [111] direction (Westwater et al., 1997, Niu et al., 2004a). Silicon nanowires grown by laser ablation
are primarily oriented in the [112] direction and seldom in the [100] or [111] directions (Tan et al., 2002).

Westwater and co-workers (1998) have shown that CVD with a high silane partial pressure produced a high density growth of thin nanowires. This is a result of a lowered effective chemical potential due to the increased silane partial pressure. This allows thinner nanowires to grow with an increased density (Westwater, et al., 1998).

The diameters of silicon nanowires grown via the VLS mechanism are known to vary with catalyst droplet size (Cui et al., 2001, McIlroy et al., 2004) and the silane partial pressure (Westwater et al., 1997). In particular, a larger diameter catalyst droplet produces larger diameter nanowires and a higher silane partial pressure decreases nanowire diameter (Westwater et al., 1998).

Silicon nanowires are grown using a range of deposition conditions and growth mechanisms. This range of conditions results in different silicon nanowire morphologies. The literature shows that the diameter and length of silicon nanowires varies greatly. Using a thermal evaporation process, silicon nanowires have been fabricated with lengths up to 4mm and with diameters of 100nm (Shi et al., 2005). Silicon nanowires have been grown by atmospheric pressure CVD with an average diameter of 100nm. These nanowires had an areal density of $3 \times 10^{17} \text{ NWcm}^{-2}$ (Kulkarni et al., 2005). Nanowires grown from atomic vapour in UHV can exhibit diameters from 3 to 7nm and lengths of up to 100nm. These nanowires tend to grow in bundles of 20 to 30nm in diameter (Marsen and Sattler, 1999). Nanowires have been grown with a range of diameters. Figure 2-9 on the next page, illustrates the number of papers from a random selection published for a range of diameters of silicon nanowires. From Figure 2-9 it can be seen that there is a greater number of publications focussing on the production of silicon nanowires with smaller diameters with a peak interest
in the nanowires with diameters below 20nm. Producing silicon nanowires with small diameters is of particular interest as the properties of the silicon nanowires diverge from that of bulk silicon to a greater extent at these small diameters. These properties will be discussed in the next section.

![Silicon nanowire diameters reported in the literature.](image)

An alternative to the more common or preferred crystalline silicon nanowires, amorphous phase nanowires have also been grown using the SLS mechanism. These exhibit a diameter range of 10-20nm and lengths of several tens of microns (Xing et al., 2003). ‘Worm like’ structures have also been grown by PECVD via the VLS mechanism (Hofmann et al., 2003) and these are likely to be amorphous silicon nanowires.
Using \textit{in situ} TEM it has been possible to observe the growth of silicon nanowires in UHV-CVD. Ross Tersoff and Reuter (2005) found that the surface of the silicon nanowire was not smooth but exhibited sawtooth facets at an angle to the direction of growth. A thermodynamic origin has been proposed for the sawtooth faceting (Ross \textit{et al.}, 2005).

The morphology of silicon nanowires is dependant on the growth mechanism and deposition technique that is used as well as the growth conditions. There is a wide range of morphologies described in the literature. The majority of research effort is in the growth and investigation of small diameter (<20nm) crystalline silicon nanowires.

\subsection*{2.5.2 Properties of Silicon Nanowires}

One of the major points of interest in investigating nanostructured and nanoscale materials is how the properties of these materials differ from that of bulk silicon.

Several groups have performed Raman Spectroscopy (RS) on silicon nanowires and compared the results to bulk silicon. One of the main items of interest is the diameter dependent downshift of the crystalline silicon peak that occurs in the Raman spectra for silicon nanowires. Silicon nanowires have been shown to have a Raman spectrum which exhibits a downshift in wavenumber of the transverse optical (TO) crystalline silicon peak in comparison to bulk crystalline silicon (Yu \textit{et al.}, 1998a). This shift has been shown to be diameter dependent (Wang \textit{et al.}, 2000, Fukata \textit{et al.}, 2005a), there is a larger shift for smaller diameter nanowires while for larger diameters the value approaches that of bulk silicon. This downshift has been attributed to the quantum confinement effect (Niu \textit{et al.}, 2004b). Yu, Bai and co-workers (1998) showed a downshift of the TO peak by 13cm\(^{-1}\) for nanowires with a diameter of 15nm. Downshifts of 10cm\(^{-1}\) for 20nm diameter nanowires (Niu \textit{et al.}, 2004b) and 9cm\(^{-1}\) for nanowires of 10nm to 100nm in diameter (Pan \textit{et al.}, 2005a) have also been reported. However, in other instances this downshift was not observed (W. S. Shi, 2000,
Zhang et al., 1998) even for nanowire diameters in the range of 3 to 43nm. It has been observed that in comparison to the peak of crystalline silicon, the silicon nanowire peak is down shifted in frequency, has a broadened line width and the line shape itself becomes asymmetric (Li et al., 1999). The asymmetric broadening in comparison to bulk silicon is often attributed to small diameters of the nanowires and the presence of defects within the silicon nanowires (Zhang et al., 1998) as well as variations in the diameter of the nanowires (W. S. Shi, 2000). Scheel and co-workers (2006) have demonstrated that the Raman spectra of nanowires are influenced by the material around the nanowires due to their low thermal conductivity. They found that the measured phonon frequency is related to the thermal conductivity of the gas (such as He or air) surrounding the nanowires (Scheel et al., 2006).

The band-gap or energy-gap is an important property of silicon nanowires that has been shown to be dependent upon the diameter of the nanowire. Ma and co-workers (2003) have shown that the energy gap increases with decreasing diameter from 1.1eV for 7nm to 3.5eV for 1.3nm which is in line with theoretical calculations made by other groups (Ma et al., 2003). The energy gap was found by using Scanning Tunnelling Spectroscopy (STS) measurements. The increase in band-gap is an indication of a quantum confinement effect within the silicon nanowires at low diameters (Ma et al., 2003). More recent theoretical work shows agreement with the results of Ma and colleagues (2003). Scheel, Reich and Thomsen (2005) have shown that the value of the energy-gap of silicon nanowires approximates that of bulk silicon for larger diameter nanowires. That is, nanowires with diameters approaching 7 to 10nm have energy gaps approaching that of bulk silicon. Scheel, Reich and Thomsen (2005) have also shown that the magnitude of the energy-gap is due to quantum confinement and depends not only on the wire diameter, but the direction of the wire axis.

A number of research groups have been able to measure the electrical properties, such as resistance, of individual silicon nanowires. Contacting the nanowires for connection to an
external circuit is difficult, often involving nanolithography and e-beam lithography techniques. The electrical characteristics of single, essentially intrinsic, silicon nanowires have been measured (Chung et al., 2000). The silicon nanowires were found to be slightly p-type (Chung et al., 2000). The creation of ohmic contacts on the nanowires is important for connecting the nanowires into devices or an external circuit. Mohney, Wang and co-workers (2004) have measured the contact resistance for p-type nanowires of 78nm and 104nm diameter and found the contact resistance to be near $5 \times 10^4 \Omega \cdot \text{cm}^2$ for Ti/Au contacts to p-type silicon nanowires. The measurements were taken using a four point technique (Mohney et al., 2005). Cui and Lieber (2001) have created silicon nanowire-based devices using crossed p-doped and n-doped silicon nanowires. The crossed p-type and n-type silicon nanowires showed good current rectification (Cui and Lieber, 2001). High density silicon nanowires grown on ITO substrates via the VLS and VS mechanisms have also been examined (Goncher et al., 2006). The Si nanowires grown by Goncher, Solanki and coworkers (2006) were doped longitudinally. The characteristics of the nanowires when measured in bulk showed a standard diode characteristic. The nanowires grown via the VS mechanism were found to have a more pronounced diode characteristic than those grown via the VLS mechanism with Au as a catalyst (Goncher et al., 2006).

The two-terminal resistance of boron doped silicon nanowires 10 to 20nm in diameter has been measured before and after thermal annealing by Cui and co-workers (2003). Before thermal annealing the resistance was an average of 160MΩ along the length of the nanowire while after thermal annealing the resistance was found to be an average of 0.62MΩ (Cui et al., 2003). This decrease in resistance was attributed to better metal-to-nanowire contacts and passivation of defects in the nanowires (Cui et al., 2003). The resistance of individual nanowires has also been measured using an in situ probing technique known as TEM-STM. The resistance of nanowires with diameters ranging from 20 to 45nm and lengths of 4.5μm was found to be 20 to 150MΩ (Erts et al., 2002). The nanowires produced by Erts and co-
workers (2002) appear to be undoped but of a larger diameter than those produced by Cui and colleagues (2003). This could account for the resistance measurements being similar despite one batch of nanowires being doped while the other is not, as the existence of dopants should render the nanowire more conductive.

The thermal conductivity of silicon nanowires has been shown to be very size dependent. Li and colleagues (2003) have conducted an experiment using silicon nanowires to thermally connect two suspended micro-fabricated microstructures. Their work showed that thermal conductance of silicon nanowires is about two orders of magnitudes lower than that of bulk silicon and that it decreases as the diameter of the nanowire decreases (Li et al., 2003).

The properties of silicon nanowires as reported in the literature are strongly size dependant. For small diameters, properties such as the band-gap change greatly from that of bulk silicon. Larger diameter nanowires have properties that tend to approximate those of bulk silicon.

### 2.6 Catalysts Used for the Growth of Silicon Nanowires

The growth of silicon nanowires often requires the use of a metal catalyst. In the VLS mechanism the role of the catalyst is to encourage the growth of single crystal silicon nanowires. The catalyst needs to be chosen carefully to achieve this outcome. For silicon to be absorbed by the catalyst it needs to be highly soluble in the chosen metal. There are a number of catalysts that are commonly used in the growth of silicon nanowires:

- The most common is gold which does not form a silicide and has a bulk Au/Si eutectic temperature that is relatively low (363°C). This results in low temperature growth and the Au does not remain (dispersed) in the Si as a fast diffusing impurity (Hofmann et al., 2003).
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- Gallium is another catalyst used, mainly in the growth of bulk Si nanowires. The main advantage of using Gallium is the extremely low bulk Ga/Si eutectic temperature (30°C) which should allow for low temperature growth of silicon nanowires (Sharma and Sunkara, 2004).

- Titanium has been used to grow silicon nanowires. However, a mechanism other than VLS is used to explain the growth of these nanowires as the growth temperature is well below the melting point of the catalyst and the bulk Ti/Si eutectic temperature. The advantage of Ti is that it does not form deep mid-band-gap levels and the solubility and diffusion coefficients of Ti are low in silicon (Kamins et al., 2000).

- Iron has been used to grow silicon based nanowires. However the deposition method used involves physical evaporation or laser ablation of an Au/Fe target (Yu et al., 1998a, Yu et al., 1998b).

- Cobalt has been used to grow silicon nanostructures via the VLS mechanism. The resulting growth is described as a ‘flower’ (Qui et al., 1999).

- Zinc has also been used to grow nanowires via the VLS mechanism. The resulting nanowires were observed to have different electrical properties from those grown with a gold catalyst under the same conditions (Yu et al., 2000).

- VLS growth of silicon whiskers, a silicon wire several hundreds of nanometres or larger in size, has also been shown to occur for catalysts including Pt, Ag, Pd, Cu and Ni (Wagner and Ellis, 1964).

- Other catalysts such as Al, In (Iacopi et al., 2007) have been used.

- As will be shown in Chapter 7, Sn can also be used as a catalyst for silicon nanowires.

The choice of the metal catalyst is also known to affect the electrical properties of resulting nanowires (Yu et al., 2000). The most common catalyst, gold, may not be the most suitable
candidate for the growth of silicon nanowires for photovoltaic applications. It is known that gold acts as a recombination centre in silicon, adversely affecting the minority carrier lifetime (S.M. and K.K., 1981) and hence device performance of a photovoltaic device produced using silicon with gold impurities. As gold may diffuse into the silicon nanowire during the growth process other catalysts, such as tin, may be a better alternative (Iacopi et al., 2007).

2.7 Substrates Used for the Growth of Silicon Nanowires
Silicon nanowires have been produced using a variety of substrates. Although most interest is devoted to what is actually being grown, the substrate used is also of interest as it can affect the ultimate usefulness of the silicon nanowires. The growth location of the nanowires can also be controlled by selective patterning of the substrate. This can be achieved by a variety of masking or lithographic techniques.

2.7.1 Substrates
Some nanowires are simply produced in bulk on the walls of tube furnaces (Shi et al., 2005) but most are grown onto crystalline silicon substrates of various orientations. This is for a number of reasons. The VLS mechanism is one of the more commonly used growth mechanisms and a gold catalyst is often used. In the VLS mechanism a metal catalyst is placed on a silicon surface and an eutectic can form. A vapour phase of silicon is then introduced into the system to produce silicon nanowires. The silicon substrate can also provide a source of silicon for the growth of silicon nanowires in both the VLS mechanism and other growth mechanisms.

The appropriate choice of crystalline silicon substrates can affect the direction of growth of the nanowires in relation to the substrate by using an epitaxial growth mechanism (Wu et al., 2002). To take advantage of the epitaxial growth mechanism the native oxide must be removed from the silicon substrate. This is not always the best approach for the growth of
silicon nanowires as there are a number of growth techniques which can benefit from an oxide layer where the oxygen from the substrate plays a role in the seeding and nucleation of the nanowires. These growth mechanisms are the oxide assisted growth mechanism and the stress driven growth of silicon nanowires. Both of these growth mechanisms use the oxide layer to produce the silicon nanowires (Prokes and Arnold, 2005, Pan et al., 2005a).

The treatment of the substrate with an HF etch to remove the native oxide layer before the addition of a gold layer is critical for epitaxial growth. It has also been found that the formation of SiO$_2$ on the gold deposited on Si(111) substrates can have a detrimental affect on the epitaxial growth of silicon nanowires (Jagannathan et al., 2006). Jagannathan and Nishi (2006) found that a HF etch after the gold deposition (3nm), and immediately before the growth of silicon nanowires to remove the silicon oxide over-layer, remarkably improved both their growth density and epitaxy of silicon nanowires.

Other substrates have also been used, such as highly-oriented pyrolytic graphite (Marsen and Sattler, 1999), ITO on glass (Huo et al., 2004) and Silicon-on-Insulator (SOI) (Gotza et al., 1998).

### 2.7.2 Patterned Growth

Silicon nanowires have been grown in selected regions of the substrates using a number of patterning techniques. A variety of lithographic techniques can be used to aid position control of silicon nanowires. These include photolithography and electron beam lithography. Both pattern the gold film used for the catalysed growth of silicon nanowires by the VLS mechanism (Wu et al., 2002). Regular arrays of vertically aligned nanowires have been grown using photolithographic techniques (Ishida et al., 2003). A SiO$_2$ mask was created and patterned on a Si(111) substrate. The resist itself was patterned by electron beam lithography and gold was deposited on the SiO$_2$ window mask. The gold on the resist could then be
removed leaving a regular array of gold dots (Ishida et al., 2003). This leads to the growth of single silicon nanowires in a regular array that can be used for field emission devices.

Nanowires produced by VLS are known to grow where the gold is deposited. By exploiting this, nanowires can be grown in patterned regions of the substrate, by placing gold nanoparticles on the surface of the substrate or by e-beam deposition of gold (Salhi et al., 2006).

A simple technique for patterning silicon nanowires into large regular arrays of nanowire clusters is by using a shadow mask during the deposition of the gold film onto the substrate (Hofmann et al., 2003, Wu et al., 2002). A TEM grid, or fine metal mesh, can be used to produce several micron-sized squares in a regular array.

### 2.8 Doping of Silicon Nanowires

To produce semiconductor devices the intrinsic silicon nanowires can be doped as either p-type, n-type or a combination of the two. Amorphous silicon can be doped during production by using phosphine and diborane as n-type and p-type dopants. Silicon nanowires grown by CVD can be doped in a similar way.

Phosphine has been used as an n-type dopant for the growth of silicon nanowires via the VLS mechanism (Wang et al., 2005). The introduction of phosphorus into the silicon nanowire as an n-type dopant was found to decrease the resistivity of the silicon nanowire. The dopant ratios used were between $2 \times 10^{-5}:1$ and $2 \times 10^{-3}:1$ phosphorus to silicon in the gas inlet stream. Structurally the nanowires consisted of predominantly single crystal silicon [111] surrounded by a thin layer of SiO$_x$ (Wang et al., 2005). Phosphine is a good candidate for the \textit{in situ} doping of silicon nanowires as it decreases their resistivity without significantly changing the morphology of the silicon nanowire.
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The use of diborane as an \textit{in situ} dopant for silicon nanowires affects the microstructure and morphology of the nanowire. The microstructure of lightly boron doped silicon nanowires does not differ significantly from undoped silicon nanowires (Pan \textit{et al.}, 2005b). At higher doping levels the wires tended to be shorter, have an amorphous silicon coating and lacked a gold tip (Pan \textit{et al.}, 2005b). The gold was found to be deposited on the outer surface of the doped silicon nanowires and this loss of gold from the tip stifled the growth of the silicon nanowire by the VLS mechanism, producing a thick amorphous silicon coating on the nanowire (Pan \textit{et al.}, 2005b).

2.9 Applications of Silicon Nanowires

Silicon nanowires are a relatively new silicon nanostructure with many potential applications in the fields of electronics, sensing, lighting and energy production. One of the more popular potential applications of silicon nanowires is in the fabrication of Field Effect Transistors (FET). Silicon nanowires have already been used to create vertical transistors as well as the more readily fabricated transistor formed when p-type and n-type silicon nanowires are overlapped. Simple p-n junctions can be formed by overlapping p-type and n-type silicon nanowires or by forming heterojunctions within the wire itself by varying the doping within the nanowire.

P-type silicon nanowire FETs have been fabricated on glass and plastic substrates by solution based assembly (McAlpine \textit{et al.}, 2003). Where deposited on a flexible plastic substrate, it was found that there was only a slight decrease in the current in the devices when they were in a bent configuration (McAlpine \textit{et al.}, 2003). Crossed nanowire UV-LEDs were assembled using a solution based approach from n-type GaN nanowires and p-type silicon nanowires on plastic substrates (McAlpine \textit{et al.}, 2003). FETs have also been fabricated by transferring silicon nanowires onto degenerately doped silicon substrates coated with silicon nitride (Byon \textit{et al.}, 2005).
Vertically aligned nanowires have been used for gated field emission devices, which have threshold voltages of 13V, that are comparable to field emission devices produced using carbon nanotubes (10V) (Ishida et al., 2003). The nanowires used were assembled at predetermined positions on the substrate using photolithographic techniques. These nanowire devices have potential applications as smart field emitter devices (Ishida et al., 2003). Cesiated silicon nanowires have been used for low-threshold field emission devices (Kulkarni et al., 2005).

Silicon nanowires have also been used as gas sensors and vapour sensors. Silicon nanowires grown between silicon electrodes experience a change in conductance when exposed to vapours containing NH$_3$ or HCl at reduced pressure (Kamins et al., 2006). In the work by Kamins and co-workers (2006) the change in current flowing through the wire was found to be dependent on the different species (NH$_3$ or HCl) being adsorbed onto the nanowires allowing the detection of the different species. Kamins and co-workers (2006) proposed that these nanowires sensors could be integrated with silicon based electronics.

Functionalising the silicon nanowires that have been grown, and integrating them with conventional silicon semiconductor electronics, leads to the potential for lab-on-a-chip devices and sensors.

An example of the application of silicon nanowires is in the detection of various biological materials such as bovine serum albumin (Shao et al., 2005). Millimetre long silicon nanowires were fabricated by an oxide assisted growth mechanism then treated with HF to remove the silicon oxide sheath from around the nanowire (Shao et al., 2005). Gold nanoparticles were then attached to the silicon nanowire by dipping in AuCl$_3$ solution before being functionalised by thioacetic acid. The nanowire strands were then attached to an insulating
plastic substrate with one end attached to a copper wire. Detection of the bovine serum albumin could then be achieved by cyclic voltammetry (Shao et al., 2005).

Silicon nanowires modified or coated with gold nanoparticles have also been used as biosensors (Yang et al., 2006). These modified nanowires were used to detect glutathione by cyclic voltammetry with good linear response and high sensitivity (Yang et al., 2006). A pH sensor has been created using functionalised silicon nanowires (Chen et al., 2006). The change in the pH of a solution was measured by the change in the differential conductance of the nanowire.

Silicon nanowires have slightly unconventional potential applications including that of self destructing systems for electronic devices. It has been shown that bulk silicon nanowires combust when a strong light is applied to the sample (Wang et al., 2003). This is due to an enhanced photothermal effect (Wang et al., 2003).

Light emitting devices are another potential application of silicon nanowires. Electroluminescence has been observed from silicon nanowires (Huo et al., 2004). The electroluminescence was generated by applying ±70V at a repetition rate of 3kHz. The electroluminescent spectrum peaked at 600nm but with no clearly defined peak, due to the size distribution of the silicon nanowires used (Huo et al., 2004).

Silicon nanowires have been used to produce addressable photodetectors using photolithography techniques for locating where the nanowires grow (Servati et al., 2007). These photodiodes consisted of essentially intrinsic silicon nanowires grown on p-type crystalline silicon substrates via the VLS mechanism. The devices showed a promising photoresponse to incident illumination (Servati et al., 2007). This bodes well for the use of silicon nanowires as solar cells.
As components in a Grätzel solar cell the electron transport properties of silicon nanowires could remove the transport bottleneck that is present within a conventional Grätzel solar cell (Wu et al., 2002).

Large area p-n junction arrays have been produced from doped crystalline silicon using an HF and AgNO$_3$ etching technique (Peng et al., 2004). The p-n junction created showed a nonlinear and rectifying behaviour with a turn-on voltage of ~1 V (Peng et al., 2004). Peng, Huang and co-workers (2004) also measured the IV characteristics of silicon nanowire arrays made of n-type silicon. They showed a rectifying behaviour likely due to the formation of a Schottky diode. Later work by this group has shown that the silicon nanowire arrays created by the etching method are suitable for photovoltaic applications (Peng et al., 2005). The nanowires were used as part of an anti-reflection coating to improve the absorption of light by the solar cell. Unfortunately the efficiency of the device was less than a similar one produced without the nanowires, due to low current collection efficiencies at the front contact (Peng et al., 2005). An analysis conducted by Hu and Chen (2007) on regular arrays of 50nm and 80nm silicon nanowires has also indicated that silicon nanowires would be useful in photovoltaics. They found that a silicon nanowire array has a higher absorption than a thin film device in the higher frequency part of the spectrum (Hu and Chen, 2007).

Tian, Zheng and co-workers (2007) have recently reported the fabrication of a single silicon nanowire based photovoltaic device. This device consists of a p-type nanowire encased in intrinsic polycrystalline silicon with a further layer of n-type polycrystalline silicon resulting in a coaxial wire type morphology (Tian et al., 2007). The nanowire was then etched to reveal the core and contacts were made to the core and outer n-layer some distance along the wire. Current Voltage (IV) characteristics of this silicon nanowire solar cell showed an open circuit voltage $V_{OC}$ of 0.26V, a short circuit current $I_{SC}$ of 0.503nA and a fill factor of 55% under AM 1.5G illumination (Tian et al., 2007). The short circuit current was found to be scaleable
with nanowire length while the open circuit voltage was maintained. Kelzenberg and co-workers (2008) have also recently produced a single-silicon nanowire photovoltaic device. Their nanowires were grown using a high temperature VLS process with a 100nm thick gold catalyst layer (Kelzenberg et al., 2008) which were used as part of a rectifying junction to act as a solar cell. The devices produced had a $V_{oc}$ of 0.19V, a fill factor of 0.4 and an efficiency of 0.46% (Kelzenberg et al., 2008). Kelzenberg and co-workers conclude that under the particular growth conditions used, a target nanowire diameter for optimal performance is $\geq 4\mu m$ (Kelzenberg et al., 2008). This is significantly outside of the range of diameters at which quantum confinement effects would be observed but may yield a more efficient device.

### 2.10 Photovoltaics

Photovoltaics has been described as the ‘art of converting sunlight directly into electricity’ (Wenham et al., 1994). Photovoltaic devices, or solar cells, are capable of using incident illumination to supply electrons to an external circuit. There are a number of different ways to produce solar cells and a range of materials from which they can be produced. Silicon is a commonly used semiconductor material for producing solid state solar cells. Solar cells produced using silicon have different properties when they are made using different types of silicon.

#### 2.10.1 History

In today’s world there is a growing demand for cheap, clean and efficient power sources. One response to this demand is the development of the photovoltaic cell.

Since the creation of the first solar cell at Bell Laboratories in 1954 much attention has been devoted to the design, production and use of solar cells. The first cell had a limited efficiency of 6% and was crystalline silicon based, as have been the majority ever since although other
crystalline semiconductor materials have been used. Laboratory cells have improved since then and are now appearing with efficiencies of 24.5% and production cells have 15-16% efficiencies (Goetzberger and Hebling, 2000).

Much of the early use of silicon photovoltaics was in power supply systems for space vehicles. However, in recent times, there is an increasing market for photovoltaics in remote area power supplies and in distributed generators on the electricity grid.

In the marketplace there are several types of solar cell technologies available including crystalline, micro-crystalline and amorphous silicon. The world market is currently dominated by crystalline silicon solar cells which held some 90.9% of the market in 2004 and 93.5% in 2005 (Singh and Jennings, 2007).

Solar cells come in a variety of designs and are made from a wide selection of materials. In the simplest form a thin film solar cell is created from several layers of semiconducting material including a p-layer, an n-layer and an i-layer to form one or more p-i-n junctions.

The semiconducting material is doped with specific dopants to create the required p-type or n-type semiconductor. A semiconductor doped with donor atoms is known as an n-type semiconductor as the charge carriers are electrons, which have a negative charge. A semiconductor doped with acceptor atoms is known as a p-type semiconductor as the charge carriers are holes, which have an effective positive charge. An i-type semiconductor, also known as an intrinsic semiconductor, is the un-doped semiconducting material.

The p-n and p-i-n junctions are simply charge-separating junctions. These separate the holes and electrons created by incident photons, in order to stop them immediately recombining. This therefore makes the electrons available for use in an external circuit. The electric field
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present within the cell moves the electrons to the n-side and the holes to the p-side of the junction (Wenham, 1994). A typical single junction thin film p-i-n solar cell can be seen in Figure 2-10, and consists of an aluminium contact, n-layer, i-layer, p-layer and a transparent conducting oxide layer.

![Diagram of a cross sectional schematic of the p-i-n junction solar cell.]

Figure 2-10: A cross sectional schematic of the p-i-n junction solar cell.

For more efficient solar cells several p-i-n junctions can be stacked together to create multi-junction cells which capture a greater amount of the light incident upon the cell. These junctions can be identical but are more often tuned to be responsive to slightly different wavelengths of light in order to absorb as much of the solar spectrum as possible.

There is still room for improvement in producing solar cells affordably. This can be done by improving the efficiency of the devices or by reducing the costs in the production. The use of novel materials, such as silicon nanostructures, could improve solar cells by combining the
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low cost of production of amorphous materials with the higher efficiency of crystalline materials.

2.10.2 Crystalline Solar Cells
Traditionally most solar cells have been made from doped crystalline semiconductors, such as crystalline silicon (c-Si). Crystalline semiconductors have a very well defined structure with both a high long range and high short range order. The characteristics of crystalline solar cells include a well defined band-gap and high quantum efficiency. However this style of cell is very expensive. It is also time consuming to make involving as it does wafers of single crystals.

These drawbacks, and the rising costs of solar grade crystalline silicon, have encouraged the development of other materials, particularly thin films, for solar cells.

2.10.3 Microcrystalline Solar Cells
Microcrystalline silicon solar cells have been created with efficiencies of up to 8.9% using a single p-i-n junction (Kupich et al., 2004) and 9% for substrate-n-i-p devices (Feitknecht et al., 2003). Microcrystalline solar cells are generally created by HWCVD and combine some of the benefits of crystalline and amorphous solar cells. They are much cheaper to make than crystalline cells and they can be used on large areas. They do not suffer from photodegradation to the same extent as amorphous solar cells. For these reasons, the use of microcrystalline silicon to produce low cost cells, is growing (Morrison et al., 2003).

The open circuit voltage of the device created from microcrystalline silicon is known to decrease linearly with increasing average crystallinity (Droz et al., 2003). Microcrystalline silicon can be combined with amorphous silicon to produce micromorph tandem cells (Shah et al., 1997, Meier et al., 2004b, Meier et al., 2004a, Feitknecht et al., 2003). Devices of this
design have been reported with efficiencies of 12% (Shah et al., 1997). This device design combines the benefits of microcrystalline and amorphous silicon to create a device with a high efficiency.

2.10.4 Nanocrystalline Solar Cells
Thin film solar cells can be produced using nanocrystalline silicon as a core component. Nanocrystalline silicon solar cells have been produced using a combination of amorphous silicon and nanocrystalline silicon in a triple junction device. This particular device had a reported initial efficiency of 14.1% and a stable efficiency of 13.2% (Yue et al., 2006). The high efficiency of this device shows that solar cells produced using thin films of nanostructured silicon can have a high efficiency.

2.10.5 Amorphous Silicon Solar Cells
The use of a-St:H photovoltaics has been increasing rapidly in recent years. The volume of worldwide sales was 34MW in 2001, a growth of 26% over the sales in 2000. However this is still only a 10% share of the total world photovoltaic market. The larger portion of the market is in crystalline solar cells due to their higher efficiencies. Even so, the growth in market share demonstrates the current interest in amorphous silicon. Single junction amorphous silicon solar cells have been produced with a 9.47% stabilised efficiency (Meier et al., 2004b) with much higher efficiencies produced in the laboratory.

Hydrogenated amorphous silicon solar cells have been in development since the late 1970s when a patent for hydrogenated amorphous silicon solar cells was received by Dr. David E. Carlson of RCA Laboratories (Wilson, 1980). Despite the length of time they have been in development there is still one major problem which is plaguing amorphous silicon solar cells. This problem is that of photodegradation or the Staebler Wronski Effect (Staebler and Wronski, 1977).
2.11 The Band-Gap in Silicon

The band-gap, also known as the optical-gap, energy-gap or mobility-gap, is an important property of semiconductors that determines the optoelectronic properties of devices created from such semiconductors. The band-gap is the minimum amount of energy needed for an electron to jump from the valence band to the conduction band as shown in Figure 2-11. For an intrinsic semiconductor, the Fermi energy ($E_F$) is located mid-band-gap and is often in the mid-band-gap states.

![Figure 2-11: Schematic of the semiconductor band-gap showing the valence band, conduction band and mid-gap states.](image)

The value of the band-gap energy ($E_g$) is characteristic for each semiconductor and it affects the optoelectronic properties of that semiconductor. For example, semiconductors are effectively transparent to photons of energy less than the band-gap energy as these photons have insufficient energy to excite an electron from the valence to the conduction band and hence are not absorbed.
The minimum room temperature band-gap energy values for some common semiconductors are:

- 1.12eV for silicon (Lide, 2005).
- 0.67eV for germanium (Lide, 2005).
- 1.35eV for gallium arsenide (Lide, 2005).

For photovoltaic devices, the band-gap energy needs to be close to the peak of the energy range of visible light (1eV to 3eV) or the spectrum of light emitted by the sun. Not all semiconductors are suitable for use as solar cells, the most suitable band-gap for which is about 1 to 1.6 eV (Wenham et al., 1994).

The band-gap in crystalline semiconductors has a much more defined edge than that of amorphous semiconductors, with few defect states within the gap. Amorphous materials tend to have broader band tails that extend further into the band-gap than those of crystalline semiconductors (Wilson, 1980). This is an inherent property of amorphous semiconductors and arises from the lack of long range structural order within the material.

Amorphous silicon semiconductors are characterised by a distribution of defect states within the band-gap. These act as traps and recombination centres and thus contribute strongly to the opto-electronic properties of the semiconductor. These localised mid-gap states arise from the tailing band edges of amorphous silicon, and defects and impurities within the structure of the semiconductor (Guha, 1982). Jackson and Amer (1982) have shown, using photo-thermal deflection spectroscopy, that in undoped amorphous silicon there is an absorption tail extending down to 0.6eV. They have also shown that this is due to silicon dangling-bond defects which exist approximately 1.3eV below the conduction band edge (Jackson and Amer, 1982). Mid-gap states can be characterised by using Deep Level Transient Spectroscopy (DLTS) (Lang, 1974). There are also some variations on this
technique including Photo Deep Level Transient Spectroscopy (PDTS) and Charge Transient Spectroscopy (QTS) (Farmer et al., 1982, Mooney, 1982). Mid-gap density of states can also be measured and characterised by a technique known as the Constant Photocurrent Method (CPM) which is a way of measuring the absorbance characteristics of a solar cell and hence the density of states (Sakata et al., 1991).

It has been observed by Longeaud (2002) that after a period of light-soaking, the band-gap of amorphous silicon semiconductors changes by a broadening of the conduction band tail into the band-gap. It was also observed that light-soaking causes the creation of states within the band-gap directly above the valence band tail (Main et al., 2004). The introduction of these states allows the absorption of photons which would otherwise be less than the energy of the band-gap and also allows the possibility of multi-photon transitions.

**2.12 Photodegradation**

A major drawback with the use of amorphous silicon to produce thin-film solar cells is the degradation of the cell’s performance after exposure to light. This is known as photodegradation or the Staebler-Wronski Effect (SWE) after Staebler and Wronski who first reported this reversible photodegradation effect in 1977. This degradation occurs over a period of exposure to light during which the photoconductivity decreases asymptotically to a minimum point at which the cell stabilizes and further exposure to light has minimal effect. The photodegradation can be reversed by thermal annealing of the cell above 150°C (Staebler and Wronski, 1977).

The exposure of a cell to light for a period of time is known as light-soaking. The purpose of light-soaking is generally to degrade an amorphous silicon solar cell to its stable state. For commercial reasons this is important so that the performance of the cell will not deteriorate after delivery to the consumer. The process of light-soaking can take many hours, so a new
degradation technique has been developed to accelerate the process (Dasgupta et al., 1998). This is a fast and reliable technique whereby the time taken to fully degrade a cell can be significantly reduced. This technique involves two phases. Firstly the cell is severely degraded by a forward current. This degrades the cell to an extent greater than ordinary light-soaking. The second phase recovers the excess degradation of the cell through a short period of light-soaking (Dasgupta et al., 1998).

The process of light-soaking causes the creation of meta-stable defects in hydrogenated amorphous silicon. It is these defects which cause the change in the cell’s performance. The main meta-stable defect introduced by prolonged light-soaking is the silicon dangling bond (Stutzmann et al., 1984). However Sakata and coworkers (1991) have observed that the change in the photoconductivity of a cell is not proportional to the inverse of the change in density of Si dangling bonds. This indicates to them that defects other than Si dangling bonds are created by prolonged light-soaking. Probable candidates are a dangling bond coupled with either an impurity or another dangling bond or both (Sakata et al., 1991).

So the process of light-soaking causes photo degradation through the creation of meta-stable defects in the amorphous silicon. The introduction of these defects degrades the photoconductivity of the cell. This degradation can be reversed through thermal annealing. The introduction of new defects is known to cause changes in a solar cell’s characteristics, such as the efficiency and the band-gap.

By introducing silicon nanostructures such as nanowires into the i-layer or p-layer of an amorphous silicon solar cell it may be possible to reduce the impact of the Staebler Wronski effect on the device’s efficiency. This reduction would result as crystalline silicon is much more resistant to photodegradation than amorphous silicon. Yet the use of nanostructures can maintain the low material costs of production.
3.1 Current Voltage (IV) Characteristics

The Current Voltage (IV) characteristic, also known as a JV characteristic when referring to current density, is a commonly used tool for analysing the electrical characteristics of a semiconductor device. IV characteristics simply show the current flows through a device as the voltage applied to it is varied. Information such as resistance and conductance can be gleaned using this technique. The characteristics of non-ohmic devices can also be examined.

To calculate the conductance of the material being measured the gradient of the IV curve is used. In the case of an ohmic conductor, this can be measured over the full curve. However, in the case of semiconductors, the conductance can be measured for different regions of the IV curve. The resistance of the material is simply the inverse of the conductance. Photoconductivity in the material can be observed by exposing the sample to a light source while the IV characteristic is being measured.

This technique is often used to analyse solar cells. It gives information on the basic electrical properties of a solar cell including the fill-factor, series-resistance, shunt-resistance, short-circuit current and open-circuit voltage, from which other factors such as the efficiency of the cell can be calculated.

The short circuit current ($I_{sc}$) is defined as the output current under illumination where the bias voltage, or the voltage applied to the sample, is zero. The open circuit voltage ($V_{oc}$) is defined as the bias voltage under illumination where the output current is zero. The maximum voltage ($V_{max}$) and maximum current ($I_{max}$) are found from the maximum power.
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point, the point on the IV curve for the illuminated cell where the product of \( V \) and \( I \) is greatest. From this information the cell efficiency and fill factor can be found.

The cell efficiency (\( \eta \)) is defined as:

\[
\eta = \frac{P_{\text{out}}}{P_{\text{in}}}
\]

(3.1)

and can be found from:

\[
\eta = \frac{I_{\text{max}}V_{\text{max}}}{AP}
\]

(3.2)

where \( A \) is the cell area, \( P_{\text{out}} \) is the power output from the cell, \( P_{\text{in}} \) is the power incident upon the cell from the source of illumination and \( P \) is the power incident upon the cell per unit area.

The fill factor (\( ff \)) is defined as:

\[
ff = \frac{I_{\text{max}}V_{\text{max}}}{I_{SC}V_{OC}}
\]

(3.3)

The current density (\( J_{SC} \)) under short circuit conditions is defined as:

\[
J_{SC} \equiv \frac{I_{SC}}{A}
\]

(3.4)

The quantum efficiency of a cell is the percentage of incoming photons that are converted to outgoing current. The fill factor is an indication of the quality of the solar cell; the higher the fill factor the closer to the ideal square IV characteristic. The fill factor is a measure of the extent to which the IV curve fills the power quadrant, in Figure 3-1 this is the quadrant of positive voltage and negative current density.

The shunt resistance (\( R_{sh} \)) of the cell is the inverse of the gradient of the IV curve as the voltage tends to \( V_{-\infty} \). The series resistance is the inverse of the gradient as the voltage tends to \( V_{\infty} \).

An example of a JV curve is shown in Figure 3-1. This shows the typical IV characteristics of an amorphous silicon solar cell.
Figure 3-1: An example IV characteristic, showing both light and dark characteristics for an amorphous silicon p-i-n junction.

IV characteristics for cells exposed to a light source are often recorded using a continuous light source. That is, the light source remains on while the current and voltage measurements are taken. Using a continuous light source has a drawback in that the prolonged exposure to light of Air Mass (AM) 1 or AM 1.5 heats the solar cell up quickly. If the cell is not properly attached to an appropriate heat-sink, thermal effects could be introduced into the data. AM 1 and AM 1.5 are standard solar spectra equivalent to what is incident on the Earth’s surface from different angles of illumination, an AM 1.5 spectrum is shown in Figure 3-2 (Wenham, 1994).

As can be seen from Figure 3-2, although the peak energy is in the region of 400nm to 800nm, the solar spectrum extends a long way into the infrared. As such, to increase the
efficiency of a solar cell, it would be useful to enhance the response of the cell to infrared illumination as there is a large amount of light in this region unexploited by conventional amorphous silicon solar cells. Also, extending into the UV region is a portion of high energy photons which could be used with nanocrystalline materials for multiple electron excitations.

A variation on the current-voltage technique is the IV flash-tester, which in a simple form uses a brief pulse of illumination during which the characteristic, or parts thereof, are measured. The advantage of this style of technique is that it reduces the amount of energy incident on the cell and keeps it from overheating as much. This is particularly important where high intensity illumination is used. The main disadvantage of the IV flash-tester is the cost of the appropriate circuitry to measure the IV characteristic in a brief period of time (Keogh et al., 2004).
3.2 Scanning Electron Microscopy

One of the major difficulties with nanotechnology and nanoscale materials arises in actually observing the material. How can the structure be observed if it is smaller than the wavelength of visible light? Electron microscopes are an answer to this question. There are two main types of electron microscopes, Scanning Electron Microscopes (SEM) and Transmission Electron Microscopes (TEM) and each has its own properties. While conventional light microscopes have a resolution in the order of ~200nm, the SEM has a resolution of ~1nm and TEM a resolution of ~0.1nm. Due to this vastly improved resolution, electron microscopes are commonly used to directly observe the morphology of nanostructured materials. An example micrograph of an aluminium coated silicon nanowire from a SEM is shown below in Figure 3-3. In this micrograph, features of less than 20nm in size can be directly observed which would not be readily visible using a conventional microscope.

![Figure 3-3: An example electron micrograph from a Field Emission Scanning Electron Microscope (FESEM) showing an aluminium coated silicon nanowire.](image-url)
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A survey conducted in 1963 about the interest in SEMs, predicted that 3-5 commercial units would be sold in the first year they were available with ten able to saturate the market place (Goldstein et al., 1975). At that time, microscopists were more interested in the higher resolution capability of the established TEM rather than the lower resolution imaging of the new SEM. The first commercial instrument was released in 1964 and was the Cambridge Scientific Instruments Mark I Stereoscan which sold 1,200 units in the US alone (Goldstein et al., 1975). Since then over 50,000 SEM units have been sold globally by a variety of manufacturers (Goldstein et al., 2003).

Scanning electron microscopy is a popular and versatile characterisation technique for a number of reasons. SEM boasts a resolution greatly exceeding that of light microscopes and other comparable techniques with figures of 1nm to 5nm routinely quoted for commercial instruments (Goldstein et al., 2003). This allows the resolution of fine detail in the specimen. Micrographs produced via this technique show a very large depth of field which allows a large portion of the specimen to be in focus on the micrograph. Because of this high depth of field, SEM produces imagery that is 3D in appearance and easy to interpret. For example, in Figure 3-3 the spiked nanowire is clearly in front of the background material. This is in contrast to the higher resolution and magnification, yet essentially two dimensional imagery, produced by a TEM. Unlike TEM, SEM allows the examination of the surface of the specimen. The use of low accelerating voltages allows the surface structure of a specimen to be observed. As the surface of the sample is generally what is of interest, bulk specimens can be used. Large specimens, provided they can physically fit within the instrument and are conductive, can be analysed. This is unlike TEM where very thin films are required which necessitates complicated sample preparation procedures.

The sample preparation required for SEM varies depending on the sample to be analysed. Conductive and solid samples such as semiconductor thin films or metal samples require
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minimal preparation, whereas biological samples require a complicated drying and coating procedure. Samples analysed in this thesis were semiconductor materials and needed minimal sample preparation for this analysis technique.

Energetic electrons are used to probe the surface of the sample. This causes characteristic x-rays to be emitted by the sample which can be collected to provide compositional information about the specimen. Recent improvements to the SEM provides the capability to determine crystal structure and orientation of crystals within a sample through the use of Electron Back Scattering Diffraction (EBSD) (Goldstein et al., 2003).

Scanning electron microscopes function by firing a finely focussed electron beam at a sample and then collecting information from the sample. The various signals emitted, and the results of electron beam interaction with the sample, are shown in Figure 3-4. The signals which are used to produce images are usually Secondary Electrons (SE) and Back Scattered Electrons (BSE) for SEM, whereas the transmitted electrons are collected for TEM. The other signals can also be used to produce micrographs if it is required and the SEM is appropriately equipped.

The primary mode of operation for the SEM is collecting the secondary electrons. These are loosely bound outer shell electrons that are provided with enough energy by the incident electron beam to be ejected from the material. When collected, these electrons provide topographical information about the sample (Goldstein et al., 2003). A secondary mode of operation involves back scattered electrons. Back scattered electrons originate in the incident electron beam. The electrons are fired at the sample and after many elastic scattering events some return to the surface and leave the sample (Goldstein et al., 2003). These can be collected to provide compositional information as the number of back scattered electrons is highly proportional to the atomic number of the material.
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Figure 3-4: Principal result of electron beam interaction with the sample (after (Griffin and Riessen, 2000)).

The elements of an electron microscope are the electron source, a series of electro magnetic lenses, apertures, signal collectors and an image capture system. A simplified schematic is shown in Figure 3-5. The electrons are fired at the sample from an electron gun which can be one of several types depending on the instrument used. The most common electron gun used on older instruments is the tungsten filament which is relatively cheap but has a shorter lifetime than many other electron sources. A higher brightness source used is a LaB$_6$ rod cathode. This has a longer life than the tungsten filaments but requires a better gun vacuum to be maintained and is more expensive (Goldstein et al., 1975). Many of the high end instruments use field emission sources which allow for a better resolution (1-5nm) and a longer lifetime but are correspondingly more expensive.
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Figure 3-5: Simplified schematic of an SEM.

The accelerating voltage also helps to determine the resolution of the SEM. The resolution in the electron microscope is limited by the wave nature of electrons. The resolution and wavelength used are related through Abbe’s equation (Griffin and Riessen, 2000):

\[ d = \frac{0.61 \lambda}{n \sin \alpha} \]  \hspace{1cm} (3.5)

where d is the resolution, \( \lambda \) is the wavelength, n is the refractive index of the medium through which the electrons are travelling and \( \alpha \) is the numerical aperture.
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The wavelength of the electron is related to the accelerating voltage:

$$\lambda = \frac{h}{\sqrt{2mqV}}$$  \hspace{1cm} (3.6)

where $h$ is Planck’s constant, $m$ the mass of the electron, $q$ the charge of the electron and $V$ the accelerating voltage (Griffin and Riessen, 2000). From this it can be seen that a high accelerating voltage will produce electrons with a smaller wavelength and hence a finer resolution.

The electromagnetic lens system is used to de-magnify, direct and focus the e-beam onto the sample. A series of scan and deflection coils are used to raster the e-beam across the sample to form an image. The final aperture controls the depth of field of the micrograph. A smaller aperture allows a greater depth of field but reduces the current at the sample by physically blocking a portion of the e-beam. Another variable that alters the depth of field and image resolution is the working distance, or the distance between the sample and the final lens pole piece. With an increased working distance the image resolution decreases but the depth of field is improved. For smaller working distances the opposite holds. At times a larger working distance may need to be used to allow rotation of the sample within the specimen chamber. A larger working distance is used to avoid potentially damaging the back-scattered-electron detector when mounted on the final lens pole piece.

The signals emitted from the sample are collected by several different types of collectors. For collecting secondary electrons an Everhart-Thornley detector is commonly used. The electrons are drawn to the detector by a metal grid with a positive bias on it. Back scattered electrons are often collected using a solid state detector (p-n junction) which is positioned around the pole piece of the objective lens. The signals from these detectors traditionally
were used to display the image on a Cathode Ray Tube (CRT) and record an image on film when required. In recent practice these signals have been captured by a computer which then manages the display and storage of the micrographs as tiff image files. The micrographs can then be analysed using analytical software to extract information, such as the size of morphological features, and printed out as required.
CHAPTER 4: EXPERIMENTAL SYSTEMS AND METHODOLOGY

4.1 Current Voltage Characteristics
The IV characteristics of the nanowire based devices fabricated in this project were measured using an existing characterisation system. IV characteristics show the current flowing through a device as the voltage applied to it is varied, allowing information about the device to be gathered, as described in Chapter 3. For this project the existing computerised measurement system at Murdoch University was calibrated and used to measure the IV characteristics of the silicon nanowire devices.

4.1.1 Experimental System
A bipolar power supply (Kepco Bipolar Power Supply/Amplifier) was used to provide a bias voltage to the cell. The current passing through the device was measured using a Picoammeter (Keithley 160B Digital Multimeter) which also contained a current to voltage converter. A computer was used to drive the bipolar power supply for the required voltage range and record the readings from the picoammeter.

The IV system was run in two modes. In the dark mode, the sample was isolated from any illumination. In the illuminated mode the cell was exposed to steady, approximately AM1 illumination provided by a 120V/300W halogen lamp. This was calibrated using a standard crystalline silicon solar cell of known properties. The system was calibrated by placing the standard cell on the sample holder and measuring the short circuit current under illumination.

The distance of the sample holder to the source of illumination was then adjusted accordingly.

The data recorded by the computer could then be used to find the resistance of the material and the presence of any photoconductance. For the photovoltaic devices produced the
efficiency, fill factor, and current density were calculated using equations 3.2, 3.3 and 3.4 respectively (page 83).

Illumination times while recording the IV characteristic were kept to a minimum to avoid any heating of the sample and contamination resulting from thermal effects.

A schematic diagram of the system can be seen in Figure 4-1. As shown, the samples were placed in a light-proof box to ensure they were exposed to the correct lighting conditions.

![Figure 4-1: Schematic of the Current-Voltage characterisation system.](image)

### 4.1.2 Experimental Procedure

To acquire the IV characteristics aluminium contacts were deposited on each of the samples to be measured. These samples included amorphous silicon solar cells, intrinsic nanowires and devices using nanowires and amorphous silicon. The contacts were then connected to the apparatus and the individual sample placed in the sample holder which was in turn placed in the dark box directly under the light source. Prior to any measurements being taken, the voltage being supplied by the bipolar power supply was zeroed.

Two sets of data for each sample were acquired. These were the light and dark IV characteristics. The data was collected and charted by a program (LabView) running on the
computer. The data collected could then be analysed to observe the device characteristics and calculate resistance, efficiency and fill factor, where appropriate.

The signal to noise ratio in the IV characterisation system is fairly low for the extremely small current measurements required in some parts of this thesis. Due to this, some smoothing of the collected IV data was undertaken when necessary for reducing signal noise. All IV curves shown in this thesis are the result of several averaged IV curves. In some cases further smoothing was required to remove or minimise signal noise. Smoothing of the IV curves was undertaken using the computer software Jandel PeakFit v4 (1995). Specifically the data was smoothed using the Savitzky-Golay (5%) algorithm (Jandel, 1995). The Savitzky-Golay (5%) algorithm was used as it effectively reduced the signal noise in the data without distorting the line shape, giving a good apparent reduction in the signal noise.

4.2 Scanning Electron Microscopy

Two microscope systems were used to analyse the silicon nanowire samples. The use of these SEMs allowed the morphology of the nanowires to be examined and measured.

4.2.1 Experimental System

Two main scanning electron microscopes were used for analysing and characterising the materials produced. The first was a Philips XL 20 based at Murdoch University, shown in Figure 4-2. This was used for finding and determining the density of nanowire growth. For higher resolution imaging, a Zeiss 1555 VP-FESEM was used. This instrument was located at the University of Western Australia. The FESEM was used for samples where surface morphology and the imaging of individual nanowires were required.
4.2.2 Experimental Procedure

The preparation procedure for the analysis of the samples under the SEM was straightforward. The nanowire samples were produced on a number of different substrates. Crystalline silicon, stainless steel and copper substrates were mounted directly to the SEM stub using double-sided, conductive carbon tape. ITO-coated glass was used for a number of samples. For mounting and analysis of these, conductive carbon tape was wrapped around
the end of each substrate before running under the substrate to connect the stub. This style of mounting can be seen below in Figure 4-3. Due to the conductive nature of the ITO, most of the sample could be readily imaged without significant charging of the sample. For non-conductive substrates such as glass, conductive carbon tape was again wrapped around the substrate before mounting on a sample stub. For these substrates, only regions near the conductive tape were measured. The nanowire film and amorphous silicon growth proved sufficiently conductive to allow clear imaging in proximity to the conductive tape.

![Figure 4-3: Silicon nanowire samples on ITO showing the method of mounting on SEM stubs.](image)

Aluminium contacts (spots) are visible on the surface.

When analysing the samples under the SEM, care was taken to take several micrographs from different regions of the sample. This was done to ensure a representative survey of the sample.

From the micrographs collected, the diameter and length of the nanowires were measured using the Gatan DigitalMicrograph 3.4 computer software package (Gatan, 1999).
Chapter 4: Experimental Systems and Methodology

calibrated line plot which showed the intensity of each pixel along the line, allowed the length and diameter of the nanowires to be determined. An example of a line profile is shown below in Figure 4-4b. It shows the width of the nanowire in Figure 4-4a to be 99nm. This method was used to measure accurately, the diameters of the nanowires.

Figure 4-4: Measuring nanowire diameter. a) An electron micrograph with the region for a line plot marked and b) the resulting plot (scale is in nm).

The density of the nanowire growth was determined by manually counting the number of nanowires per square micrometer of the sample from a number of micrographs. Counting the density of the nanowires was only possible for samples where the nanowires were relatively free of growth defects and the tip, or preferably both ends, of the nanowire was visible. For some micrographs, counting the nanowires was not possible as many of the nanowires were coiled, exhibited many growth defects or the ends were not visible. In this situation the coverage of the sample was calculated. This was done by determining the portion of each micrograph covered with nanowires and taking an average across the micrographs of the sample to calculate a representative figure. The coverage for each micrograph was found by inspecting the digital micrograph, selecting the background (substrate), converting to black and then measuring the proportion of the image that was not black using a histogram of the micrograph.
To measure the number of growth defects or number of kinks/cm² of the sample, the visible growth defects were manually counted. The growth defects were very evident in gold-catalysed samples as the nanowires changed direction abruptly. Several growth defects or kinks can be seen in Figure 4-4a. As in the case with the nanowire density, this measurement was averaged over the micrographs collected for the sample to provide a representative figure.

### 4.3 Deposition System

A versatile custom-built deposition system is available at Murdoch University for the deposition of silicon thin films. The deposition system allows the use of CVD, PECVD and HWCVD for the production of amorphous silicon, microcrystalline, nanocrystalline and nanostructured silicon. The growth of silicon nanowires was deemed within the capabilities of the pre-existing PECVD chamber via conventional CVD growth or plasma-enhanced growth.

The deposition system at Murdoch is a two chamber design with a PECVD chamber (Lund, 1993) and HWCVD (Mohamed, 2004) chamber interconnected by an airlock. Samples can be transferred from one chamber to the other using a magnetic transfer mechanism (Mohamed, 2004). A photo of the twin chambers and transfer equipment can be seen in Figure 4-5.
This PECVD system can be used to produce amorphous silicon by plasma enhanced or glow discharge CVD or conventional chemical vapour deposition. The system consists of a stainless steel chamber 20.2 cm in diameter and 20.5 cm high. There are a number of ports and flanges for the connection of gas handling, view ports and instrumentation feed-throughs into the chamber. This chamber is connected via a gate valve to an airlock and transfer mechanism which allows the changing of samples without breaking the vacuum within the chamber. The HWCVD chamber is also connected to the airlock and transfer mechanism by a second gate valve. Each chamber can be operated independently without cross-contamination of materials. The two deposition chambers share common gas handling apparatus but are pumped separately. Each chamber has a heater in the upper flange which is monitored and controlled by independent thermocouples and heater controllers.
4.3.1 Plasma Enhanced Chemical Vapour Deposition (PECVD)

This PECVD chamber is of the parallel plate RF variety. The sample holder, shown in Figure 4-6, is attached to the top heater block by a set of rails which can either be bolted down for good thermal contact, or left loose to allow the use of the sample transfer mechanism. The stainless steel substrate holder and heater block form one electrode (the ground) of the system. The RF power is supplied to an insulated circular plate electrode that is usually 15mm beneath the heater block. The 13.56 MHz signal used in this system to produce a plasma, is generated by a commercially available CB transceiver (Kenwood TS-43X which was replaced with an ICOM 710 part way through the project). This is capable of power output of up to 100W; though in practice much lower powers are normally used. The carrier wave only mode is used for PECVD. The signal from the generator is passed through a RF wattmeter (Bird 43) to measure signal power. An impedance matching circuit is located between the wattmeter and the chamber itself and is used to minimise the reflectance of the signal. It can be varied to properly match current system conditions. When in use for the deposition of amorphous silicon, the plasma was struck at a power of 9W before being reduced to between 3W and 4W.

Figure 4-6: The stainless steel sample holder used in this work.
4.3.2 Pulsed PECVD (PPECVD) Modifications

During this work it was found that a variant of the PECVD technique, which is known as Pulsed PECVD or (PPECVD), could be useful for the growth of silicon nanowires.

The modification of the existing PECVD system to include pulsed capabilities was fairly straightforward due to the use of a consumer CB radio. A pulse generator (SRS Model DG535) was attached to the microphone input of the CB transceiver which was then switched to AM (amplitude modulation) mode. By producing a square wave pulse on the pulse generator and feeding it to the input of the CB radio, the RF signal was modulated. A range of frequencies and mark space ratios could be produced using the pulse generator. A digital oscilloscope (Tektronix TDS 220) was also attached to the pulse generator, as well as a small antenna placed near the chamber, to compare the square wave pulse to the actual RF signal.

4.3.3 Pumping and Gas Handling

Each deposition chamber is independently pumped by a diffusion pump that is backed by a sealed Pfeifer two-stage rotary pump. This diffusion-pumped system gives a system base pressure of approximately $10^{-6}$ torr. The chambers are pumped down from atmospheric pressure via a third, air-only, two-stage rotary pump, which is also connected to the airlock. The diffusion pumps use an inert synthetic oil (FOMBLIN 18/8) to avoid contamination of the main chambers. The silane rotary pumps are backfilled with argon to prevent oxidation of silane within the pump.

The gas handling system is shown in Figure 4-7 along with the pumping system and small system schematics of the PECVD and HWCVD chambers. A range of reactant gases can be connected to the deposition systems. These include silane, germane, diborane, phosphine, methane, ammonia, hydrogen and argon.
The gas piping shown above in Figure 4-7, connects the gas bottles via a series of electronic flow meters to a common manifold. There are non-return valves between the silane and dopant gases (diborane and phosphine) to add safety to the system. The proportions and
flow-rates of the various gasses are controlled by the mass flow controllers into the common manifold. The gases are mixed to the correct ratio in the manifold before being fed into the PECVD or HWCVD chamber. Each of the gas lines and the manifold can be individually evacuated and purged using argon. This was done several times both before reactant gasses were introduced and after they were removed. Before each deposition, the gas lines, manifold and chamber are individually flushed and purged with argon to remove contaminants. After the deposition, the chambers and lines were again flushed and purged to prevent cross contamination, and to bolster system safety. Any remaining gas in the system was evacuated using the silane rotary pump.

4.4 Substrate Preparation
A variety of substrates were used during the course of this work including aluminosilicate glass, ITO coated glass, polished stainless steel, polished copper and crystalline silicon of different orientations. The substrates were cut to fit the sample holder, Figure 4-6, used in the deposition system to sizes of 1x1 cm for crystalline substrates, 1x2 cm for metal substrates and ~1.5x5 cm for glass substrates. All substrates were cleaned before other treatment by the same procedure. The substrates were all cleaned by an ultrasonic bath using decon-90, ultra-pure water and propanol with 5 minutes per each step. After a final ultra-pure water rinse the substrates were dried using high-purity nitrogen before being subjected to further treatment.

4.5 Metal Coating
A thermal evaporation system, shown in Figure 4-8, was used for coating substrates and samples with various thicknesses of metals. This system is pumped to vacuum by a two stage rotary pump and a turbo-molecular pump. The required metal such as gold or aluminium was placed in either a tungsten boat or upon a coiled tungsten filament which was attached to two electrodes within the system. Samples were placed inverted on a framework above the filament allowing the use of shadow masking if required. For the production of photovoltaic
devices, a mask consisting of a series of equal-sized holes is used for aluminium coating. This allows a number of contacts to be made to the one sample. A shutter is located between the filament and the samples. For deposition, the system was evacuated to a pressure in the order of $10^{-5}$ torr. Once this pressure was reached, a current was passed along the filament heating the metal to the point where it evaporates. The shutter was then opened and the metal was allowed to coat the samples. The shutter is used to block the first amount of metal evaporated from the filament to avoid contamination by any low boiling point impurities in the metal. After the required amount of metal was deposited, the shutter was closed and the system returned to atmospheric pressure.

A quartz crystal microbalance can be used \textit{in situ} to measure the thickness of the metal coating on the samples. The frequency change between a probe crystal and a reference crystal is used to calculate the thickness of the metal coating with nanometre precision.
5.1 Introduction

The first step to producing silicon nanowire based solar cells involves the production of silicon nanowires. There is a large amount of information in the literature about the growth of silicon nanowires using various techniques. The various recipes used by different groups were analysed to provide the basis of a recipe to produce silicon nanowires on the CVD and PECVD systems available at Murdoch University. There are a number of variables that affect the growth of silicon nanowires. These variables needed to be optimised for the existing deposition system in order to produce high density films of small diameter, high aspect ratio silicon nanowires. High density films of silicon nanowires needed to be grown to allow the production of the silicon nanowire thin film devices that will be presented in Chapter 11.

In this work, silicon nanowires have been grown using PECVD at temperatures below the eutectic point of gold and silicon. Thermal CVD was also used at the same temperatures to examine the advantages of using PECVD in the fabrication of silicon nanowires. A gold catalyst was tested as it is commonly used and does not form a metal silicide (Hofmann et al., 2003).

This chapter details the role in nanowire growth of temperature, chamber pressure and the role of the presence, and duration, of a silane plasma. How these factors affected the growth characteristics and morphologies of the silicon nanowires is also detailed. An investigation of the effects of these growth parameters using scanning electron microscope (SEM) images is presented. By employing a plasma during the deposition it was anticipated that lower deposition temperatures could be used, potentially allowing the use of materials with a low
melting point as substrates. From the observation and study of the effect of these parameters, the growth, density and morphology of the nanowires should be able to be controlled for future depositions.

5.2 Experimental Details
Polished n-type Si(100) substrates were used for all samples. They were cleaned, as detailed in Chapter 4, and coated with gold (99.99%) catalyst layers of thicknesses varying between 0.8nm and 45nm. The samples were loaded into the PECVD chamber and mounted on the heater block. The samples were heated to the desired temperature in the presence of argon (2.7 torr) for 35 mins. The argon was then evacuated and replaced with 100% silane (SiH₄) and allowed to heat for a further 15 mins. Changing the gasses within the chamber tended to lower the substrate temperature. This extra period of time was used to return the samples to the desired temperature after the gas change over. The silane pressure during deposition was varied between 0.55 torr and 2.7 torr depending on the pressure to be investigated. The sample temperature was varied between 220°C and 335°C. A range of plasma variations using a 13.56 MHz RF signal were trialled. This included single plasma pulses of durations between 1s and 45 mins. The duration of thermal CVD following the plasma pulse varied from 0 mins up to 90 mins.

The morphology of the samples was investigated by scanning electron microscopy (Phillips XL20 and Phillips XL30).
5.3 Results

The growth of silicon nanowires is affected by a number of conditions. Under the VLS mechanism the parameters having the greatest affect on the growth of silicon nanowires are:

- The thickness of the catalyst layer.
- The substrate temperature during deposition.
- The pressure of the source gas during deposition.
- The type or existence of plasma in the PECVD variant of the VLS mechanism.

The duration and type of plasma in PECVD variants is an important parameter, especially at lower substrate temperatures.

5.3.1 Plasma

A PECVD chamber was used in the deposition of silicon nanowires. The use of a gas plasma is known to increase the deposition rate of silicon nanowires (Hofmann et al., 2003). However the catalysed growth of silicon nanowires is not dominant over the un-catalysed growth of amorphous silicon (Hofmann et al., 2003).

The role of plasma was investigated by using a range of plasma assisted growth durations. This involved starting and maintaining a gas plasma for a period of time, between one second and five minutes, during the deposition.

It was found that, to ensure growth of silicon nanowires where a silane partial pressure of 2.7 torr and a substrate temperature of 335°C were used, a gas plasma was needed. For a deposition time of 90mins without any silane plasma there was no occurrence of nanowire growth. For plasma times in the order of 5 minutes, followed by 85 minutes of thermal CVD, SEM images showed only a rough surface, indicative of an amorphous film coating the
substrate. Plasma durations between 1 second and 15 seconds yielded nanowire growth. Figure 5-1 shows SEM images from a sample with 1 second of plasma and a sample with 5 second of plasma. Both samples show similar length wires of 2µm to 4µm. This indicates a high growth rate of greater than 2µms$^{-1}$ for silicon nanowires when PECVD is used. It also indicates that under these growth conditions, the nanowire growth may take place primarily when the plasma is first struck, or turned off, as the overall nanowire length is independent of the plasma assisted deposition time.

![Figure 5-1: Similar length wires are produced by different durations of plasma a) 1 second and b) 5 seconds.](image)

### 5.3.2 Temperature and Pressure

The deposition temperature is an important parameter for the successful nucleation and growth of silicon nanowires. The VLS mechanism indicates that the catalyst layer must be a liquid for growth to occur. As the eutectic point of gold and silicon is 363°C, nanowire growth would not normally be expected to occur below this point. However, it has been shown that silicon nanowires can be grown at 320°C via the VLS mechanism (Westwater et al., 1998).

The deposition pressure is known to affect the morphologies and growth of silicon nanowires. At higher silane partial pressures, the wires become thinner and grow with greater
density (Westwater et al., 1998). Also, at higher pressures and lower temperatures, the nanowires exhibit growth defects such as kinking.

Nanowire growth was found to be denser at higher chamber pressures. At low pressures it was found that very few nanowires grew and at a much lower density. However, only a few different chamber pressures were tested. For nanowire growth, the pressure in the PECVD chamber is currently optimised at 2.7 torr. For this reason the majority of samples mentioned in this paper were deposited at 2.7 torr.

A range of depositions were conducted at substrate temperatures between 210°C and 335°C. The temperature of the substrate relative to the temperature of the heater block was checked with the use of thermocouple probes. The probes were alternatively mounted in the sample holder directly or spot-welded to a piece of stainless steel that was placed where the silicon samples were mounted. It was found that nanowires could grow at 320°C and that below this temperature observations indicated no nanowire growth. The nanowires grown at 320°C, compared to those grown at higher temperatures, were much thicker (560nm), were very short (940nm) and were likely to be amorphous rather than crystalline (Figure 5-2a). The wires grown at 335°C had diameters on the average of 130nm with some wires as thin as 60nm. The length of the wires grown at 335°C was up to 6µm. These wires also exhibit growth defects such as kinks which indicate they are likely to be crystalline silicon (Figure 5-2b). For the examples in Figure 5-2 the depositions consisted of a 5s plasma pulse followed by 90 minutes of thermal CVD.
5.3.3 Catalyst Layer

A gold layer was used as a catalyst for nanowire growth because of the relatively low eutectic point of gold and silicon (363°C). The VLS mechanism indicates that a liquid catalyst is needed for nanowire growth to occur (Wagner and Ellis, 1964). As a nanowire is grown from the liquid catalyst droplet, the diameter of the nanowire is determined by the diameter of the catalyst droplet (Cui et al., 2001). The size of the liquid catalyst droplet, when the sample is heated to the deposition temperature, is determined by the thickness of the catalyst layer deposited on the substrate (Wu et al., 2002).

To examine how the gold catalyst layer thickness affected the diameter of the silicon nanowires produced under an optimised set of deposition conditions, a series of samples was prepared with a range of catalyst layer thicknesses. The thickness of the layer was measured by a Quartz Crystal Microbalance (QCM). The thickness was varied between 0.8nm and 45nm. The deposition conditions were kept identical for this series of depositions. The chamber pressure used was 2.7 torr and the substrate temperature was maintained at 335°C. The depositions consisted of a 5 second plasma pulse followed by 90 minutes of thermal CVD.
Chapter 5: Growth Conditions and Optimisation

From the SEM images of the samples it was observed that, under these growth conditions, no nanowires nucleated on the substrate for gold thicknesses below 1nm and very few grew for layers less than 5nm. For gold thicknesses between 10nm and 45nm, numerous silicon nanowires were observed, the greatest density being near 25nm (Figure 5-3). The higher density growth can be seen in Figure 5-3c, for a sample with a 24nm catalyst layer.

![SEM images of different catalyst layer thicknesses](image)

*Figure 5-3: Nanowires grown from different catalyst layer thicknesses a) 9nm, b) 20nm c) 24nm and d) 31nm.*

From the SEM images, the average diameter of the silicon nanowires could be measured. It was found that there was an almost linear dependence of the average diameter of the silicon nanowires on the thickness of the initial catalyst layer as shown in Figure 5-4. However it must be noted that there are some variation of nanowire diameters within the one sample.
Figure 5-4: The variation of average diameter of the as grown silicon nanowires with Au layer thickness.

For nanowire growth to occur, the gold catalyst needs to be present. Figure 5-5 shows that beyond the edge of the gold film, as deposited through a mask, no nanowire growth occurred. This is shown by the increased density of silicon nanowires towards the lower right corner of Figure 5-5, whereas the silicon substrate can be seen in the upper left corner.
5.4 Discussion

Under optimal conditions, the silicon nanowires grown had an average diameter of less than 100 nm and a length of up to 6 µm. The optimum growth conditions of those tested in this work, were where the observed density of the nanowires was greatest, the diameter was small and the aspect ratio of the silicon nanowire was large. Optimal conditions consisted of a substrate temperature of 335°C, chamber pressure of 2.7 torr and a plasma duration of 5 seconds followed by 90 minutes thermal CVD. The wires often exhibited growth defects such as kinks which indicated that the nanowires were crystalline. Some amorphous wires were also observed. These tended to have worm-like structures and have a larger diameter as shown in Figure 5-6. The morphology of the nanowires depicted in this paper is similar to that demonstrated by other groups albeit these nanowires have a larger diameter (Hofmann et al., 2003).
The growth mechanism invoked for these nanowires is the VLS mechanism. Figure 5-5 demonstrates that the gold catalyst needed to be present for silicon nanowire growth to occur. It can be seen that there were no nanowires grown on the portion of the substrate without gold film on it. Further support for the VLS mechanism can be seen in Figure 5-6, where the amorphous nanowires have the characteristic bright tip. This indicates the presence of the gold catalyst on the end of the nanowire not attached to the substrate.

**Figure 5-6: Amorphous nanowires that demonstrate the characteristic gold tip of the VLS mechanism.**

### 5.4.1 Plasma

It was found that for short plasma durations, numerous silicon nanowires nucleated and grew. For longer durations fewer nanowires grew on the samples. When a silane plasma was used both silicon nanowires and amorphous silicon are produced. There was no particular preference for silicon nanowires to grow. As a result, if the deposition rate of amorphous silicon is too great, nanowire growth can be smothered. This occurs when the liquid catalyst
droplet is coated in a layer of amorphous silicon produced from the silane plasma. This halts
the absorption of the silicon from the source gas into the catalyst droplet thus limiting the
growth of silicon nanowires under these conditions. Alternatively, the nanowires growing
parallel to the substrate surface become buried in amorphous silicon resulting in a textured
surface with few nanowires being visible to the SEM. Thus under the growth conditions
used, a short plasma pulse in the order of seconds, tends to encourage the growth of silicon
nanowires. In comparison, longer plasma durations tend to reduce nanowire nucleation and
swamp nanowire growth with amorphous silicon. When no plasma was used, nanowires grew
but rarely. This indicated that the plasma is needed for nanowire growth under the growth
conditions used. This does agree with the work done by Hofmann and co-workers (2003)
which indicates that the use of plasma enhances the growth rate of silicon nanowires.

For plasma durations of both 1 second and 5 seconds, it was found that silicon nanowires
with similar diameter, length and density were produced. This demonstrates that, under the
growth conditions used, the average length of the nanowires is independent of the plasma
duration. This indicates that the nanowire growth may occur primarily when the plasma is
first struck or turned off. This could possibly be due to localised substrate heating due to
current flow when the plasma is struck or turned off. The effect of increasing the number of
times the plasma is struck and turned off within the deposition is investigated further in
Chapter 6. A fixed deposition time will be used with a varied pulse frequency to alter the total
number of times the plasma in struck and turned off.

### 5.4.2 Temperature and Pressure

During the production of these silicon nanowires it was found that temperature in particular
had a significant influence on the nucleation and growth characteristics of the nanowires. It
was found that growth could occur below the eutectic point of gold and silicon. However, at
temperatures significantly below the eutectic point there was no occurrence of nanowire
growth. This was not unexpected as, under the VLS mechanism, a liquid catalyst is required. Therefore the substrate temperature needs to be close to the eutectic point, or preferably above it. However, it has been shown that the size of a particle affects its melting point. Nanoscale particles have a lower melting point than the bulk material. Due to this, nanowire growth can occur below the bulk eutectic point of gold and silicon. The temperature of the substrate may also be affected by heating due to the presence of a gas plasma. It has previously been shown by Westwater and co-workers (1998) that silicon nanowires can be grown via thermal CVD at temperatures as low as 320°C. However, the deposition pressure used by Westwater and co-workers (1998) was 10 torr (10% silane in He) rather than the 2.7 torr (100% silane) used here. A different method of substrate heating was also employed (Westwater et al., 1998). To successfully grow high density nanowires a substrate temperature close to, and preferably above the melting point of the catalyst, is needed. A higher temperature produces nanowires more readily.

It was found that at higher pressures (2.7 torr) the density of nanowires grown on the silicon substrate was significantly greater than those grown at lower pressures (0.9 torr). It was found that a higher pressure produced thinner nanowires with a greater density. This is a similar result to that found by Westwater and co-workers (1998). They indicate that this is a result of a lowered effective chemical potential due to the increased silane partial pressure. This allows thinner nanowires to grow with an increased density. Thus, for high density growth of thin nanowires, a higher silane partial pressure is preferable.

5.4.3 Catalyst Layer
The thickness of the catalyst layer was found to have an affect on the diameter of the silicon nanowires. It was found that thicker catalyst layers produced nanowires with a larger average diameter. It is known that the diameter of a silicon nanowire grown via the VLS mechanism is determined by the diameter of the catalyst droplet as the silicon nanowire is extruded from
the liquid catalyst droplet (Cui et al., 2001). The size of the droplet is determined by the amount of gold catalyst deposited on the surface which is controlled by the thickness of the catalyst layer (Wu et al., 2002).

Observations were made of the silicon nanowires produced using the growth conditions mentioned earlier and using varying gold layer thicknesses. It was noted that very few nanowires grew from catalyst layers of a thickness less than 5nm and none grew for catalyst layer thicknesses below 1nm. This was slightly unexpected as results by Hofmann and co-workers (2003) show that nanowires were grown using a similar process with catalyst layer thicknesses of 1nm and 0.5nm. It was also found that under the growth conditions described in this chapter, the optimum gold catalyst layer thickness was in the order of 25nm. This produced silicon nanowires with a small diameter and at reasonable densities.

With PECVD, the growth conditions used and a relatively low substrate temperature, a thicker gold layer may be needed for the catalyst droplets to form. However, if the catalyst layer was in the order of 45nm, it was found that fewer nanowires grew. This was possibly due to the catalyst amalgamating into large clusters, or the formation of large regions of gold silicon alloy.

The average diameter of silicon nanowires can be controlled by varying the catalyst layer thickness. At very low thicknesses insufficient catalyst droplets of the appropriate size, as governed by the Gibbs-Thomson effect (Westwater et al., 1998), were present to allow nanowire growth to occur via the VLS mechanism. Varying the catalyst layer thickness also had an impact on the density of the silicon nanowires.

**5.5 Conclusions**

It has been demonstrated that silicon nanowires can be grown at substrate temperatures at 335°C using a PECVD system. The role of the plasma was to trigger the nucleation of the
silicon nanowires and increase the growth rate. It was found that a short plasma pulse encourages the growth of silicon nanowires while longer plasma pulses tend to coat the substrate in amorphous silicon.

Temperature was found to be an important growth parameter. Temperatures nearer the eutectic point of gold and silicon were more favourable to nanowire growth than temperatures significantly below this point.

As the VLS mechanism was used to deposit silicon nanowires in this work, the role of the catalyst layer was investigated. It was found that the average diameter of the silicon nanowires could be controlled by controlling the catalyst layer thickness. Additionally it was found that for thin gold layers, very few nanowires nucleated. This was possibly due to the lack of sufficient liquid catalyst. Equally, thick layers produced less silicon nanowires, possibly due to agglomeration of the gold-silicon eutectic material in regions of the substrate.

It has been found that silicon nanowires can be grown using the existing deposition system at Murdoch University. By using a PECVD approach to the growth of silicon nanowires it was anticipated that the growth rate and deposition conditions can be varied to allow the growth of silicon nanowires of high aspect ratio at temperatures below the eutectic point of gold and silicon. Although the thickness of the gold catalyst layer did affect the growth density of the silicon nanowires, other deposition conditions need to be optimised to improve the overall growth density of the nanowires. The highest density of silicon nanowires was produced when a 25nm gold film was used. However, using PECVD the density of the silicon nanowires and overall portion of the sample covered with silicon nanowires was inadequate for producing thin film nanowire devices.
6.1 Introduction
The silicon nanowires produced, as described in Chapter 5, were not of sufficient growth density or sample coverage to warrant producing devices. Building on the initial results in Chapter 5, other deposition techniques needed to be explored that could increase the density or growth rate of the silicon nanowires. One such variant which is used in the production of a-Si, nc-Si and μc-Si to increase the deposition rate is Pulsed PECVD. This technique suppresses the dust formation that tends to occur when the deposition rate is increased simply by increasing the plasma power. (Das et al., 2003). To test this technique on the growth of silicon nanowires, the necessary modifications were made to the deposition system as described in section 4.4.2.

This chapter aims to determine the affect of PPECVD on the growth rate and morphology of silicon nanowires grown using PPECVD via the VLS mechanism. This is examined over a range of modulation frequencies. The addition of a pulsed plasma could lead to higher deposition rates or a denser and more uniform growth of silicon nanowires due to the suppression of dust formation and the higher deposition rate generated by PPECVD.

6.2 Experimental Details
Polished n-type Si(100) substrates were used for all samples, they were cleaned and coated, as detailed in Chapter 4, with gold (99.99%) catalyst layers of 100nm. Gold was chosen as it is a catalyst often used to grow silicon nanowires since the eutectic temperature of gold and silicon is 363°C. However, the eutectic point is known to decrease for nanoscale materials by a few tens of degrees. This allows the use of temperatures such as 335°C. This was within the region the heater on the deposition system could reach. Results in Chapter 5 indicated that
25nm films of gold produce a good crop of nanowires. However some preliminary PPECVD results showed an improved density for 100nm gold films. Although 100nm catalyst layers produced nanowires with a larger diameter the density was much improved. For this reason 100nm catalyst layers are used as a standard for much of the following work.

The catalyst coated samples were loaded into the PECVD chamber and mounted on the heater block. The samples were heated to 335°C for 35 minutes in the presence of 3.0 torr of argon. The argon was then removed and silane at 3.0 torr was introduced into the chamber. The system was allowed to stabilise for a further 15 minutes before the deposition commenced.

A square wave generated by a pulse generator (SRS Model DG535) was used to modulate the 13.56MHz signal which generated the plasma. Only square wave modulation was examined in this work. A range of modulation frequencies between 125Hz and 1000Hz were tested and the mark space ratio was held at a constant ratio of 1:1. The deposition time, for each of the modulation frequencies and catalyst thicknesses used, was maintained at 5 seconds or 10 seconds with plasma. This was followed by a 10 minute interval of CVD growth without the presence of the plasma. Following this, the system was purged and evacuated.

Once the chamber was cooled to room temperature, the samples were removed and mounted on Scanning Electron Microscope (SEM) stubs for measurement. The samples were analysed using a Phillips XL20 SEM.

**6.3 Results**

The presence of a pulsed plasma during deposition, at any of the frequencies used, created a sample with a greater overall coverage of nanowires. That is, nanowires were found to grow
all over the substrate rather than in limited areas of the substrate. This coverage also tended
to increase with the frequency used.

Under the growth conditions used, the temperature of the substrate can vary across its
surface. The substrate was placed in a stainless steel substrate holder (Figure 4-6) which was
bolted directly to the heater block in order to hold the substrate snugly against the heater.
However, the centre of the substrate can often be cooler than the portions in direct contact
with the substrate holder. This led to nanowire growth in limited areas of the substrate,
towards the edges, as shown by the different coloured bands in Figure 6-1b and the density
of growth regions in Figure 6-1a. Using the pulsed plasma it was found that the nanowires
tended to grow over larger areas of the substrate, particularly for higher modulation
frequencies. In most samples this resulted in an even growth across the portion of the
substrate coated in gold as shown in Figure 6-1c and d.

Figure 6-1: Silicon nanowire films on silicon substrates grown using different pulse frequencies: a) no
pulse, b) 125Hz, c) 500Hz and d) 1000Hz.
Chapter 6: Pulsed PECVD for the Growth of Silicon Nanowires

The increase in coverage can be seen in Figure 6-1. This shows a series of photographs of the substrates. The substrates pictured are 1cm² pieces of crystalline silicon. Figure 6-1a shows the patchy growth of silicon nanowires grown at 335°C with a plasma time of 5 seconds with no pulsing on a 100nm gold coated substrate. The nanowire growth is evidenced by the gold-orange coloured spots scattered across the substrate with a higher density towards the edge of the gold film on the top and left of the image where the contact with the substrate holder was greatest. Figure 6-1b used the same growth condition with the addition of a pulsed plasma at 125Hz. It can be seen that the nanowire film covers a large portion of the substrate in comparison to the sample deposited without pulse modulation, as demonstrated by the colouration of the film. Figure 6-1c and Figure 6-1d show the samples produced using 500Hz and 1000Hz respectively. A more uniform growth across the gold coated portion of the substrate is evidenced by the even colouration of the film.

A series of SEM micrographs was taken of each sample and the morphology and density of nanowire growth were measured. As there was some variation in the density of silicon nanowires in differing regions of a single sample, an average across several images of various locations on the sample was taken. It was found that the number of nanowires (NW) per µm² increased with the increase in plasma modulation frequency.
Figure 6-2: The increase in nanowire density for increasing plasma modulation frequency.

Figure 6-2 shows the increase in average nanowire density with increasing plasma modulation frequency. The density ranged from 0.34µm$^{-2}$ for the samples produced using un-modulated plasma to 0.65µm$^{-2}$ for the samples produced with a modulation frequency of 1000Hz.
Chapter 6: Pulsed PECVD for the Growth of Silicon Nanowires

The average diameter of the nanowires was measured for each of the pulse frequencies used. It was found that there was no notable change in nanowire diameter (Figure 6-3) with an increase in plasma modulation frequency. The average nanowire diameter for nanowires grown using a 100nm thick gold catalyst layer was 150nm. The nanowires were observed to have a constant diameter throughout their length.

The upper image (secondary electron detector) in Figure 6-4 shows typical nanowire growth of moderate density. The lower image (back scattered electron detector) clearly shows that gold is present on the tips of the silicon nanowires. This is highlighted by the bright dots on the end of the nanowires. This indicates that the growth mechanism used to produce the silicon nanowires was the VLS mechanism.
6.4 Discussion

It was found that the average density of the nanowire growth increased with increased plasma modulation frequencies under the growth conditions used. This increase is quite distinct as seen in Figure 6-2. The coverage of the sample by the nanowire film was also found to improve with the use of a pulsed plasma and tended to improve with an increase in plasma modulation frequency. This trend can be seen in the photos in Figure 6-1. The photos also show the colours that a silicon nanowire film of high density tends to produce. These are mainly a dull gold-orange colour. The density of nanowires grown in this work is greater than the densities of nanowires grown by other groups. They obtained nanowire densities of 0.3µm\(^2\) (Kulkarni et al., 2005) although under vastly different growth conditions.
Chapter 6: Pulsed PECVD for the Growth of Silicon Nanowires

The nanowire density for the unmodulated plasma in this chapter was 0.34µm\(^{-2}\) which increased to 0.65µm\(^{-2}\) for the plasma modulated at 1000Hz.

Both the increase in sample coverage, and nanowire density, are proposed as being due to the increase in the number of times the plasma is struck and turned off during the deposition process. Previous work (Parlevliet and Cornish, 2005) has shown that differing plasma durations yield similar nanowire growth. This previous work was conducted using similar growth conditions to the current work with the exception that the silane plasma was turned on and off manually. This work indicated that under the growth conditions used, the nanowire growth occurred primarily when the plasma was first struck or turned off, i.e. under transient conditions. Steady state conditions do not appear to favour nanowire growth to the same extent. Hence an increase in the number of times the plasma is struck or turned off improves the growth of silicon nanowires under these conditions. The improvement in growth could be due to heating of the substrate by a current induced by the repeated striking of the plasma. It has been shown that the growth rate of silicon nanowires improves with increasing temperature (Kikkawa et al., 2005). The slight heating of the substrate by a repeatedly induced current would increase the temperature of the centre of the substrate to conditions more favourable to nanowire growth.

Another possibility is that the conditions in the steady state RF plasma are not optimal for the growth of silicon nanowires. A better set of conditions occurs during the start-up and extinguishing phases of the plasma. These conditions may only be transitory, but by repeatedly cycling through them, improved nanowire growth or improved nanowire nucleation is achieved.

PPECVD is known to increase the deposition rate of a-Si, nc-Si and µc-Si while suppressing the dust formation that tends to occur when the deposition rate is increased simply by
increasing the plasma power (Das et al., 2003). It has also been previously shown that the use of a silane plasma increases the growth rate of silicon nanowires (Hofmann et al., 2003). From this it follows that the use of PPECVD should yield an improved crop of silicon nanowires.

The diameter of the silicon nanowires grown using PPECVD did not exhibit any notable changes with an increase in plasma modulation frequency as seen in Figure 6-3. The role of a plasma in silicon nanowire deposition is to increase the growth rate of silicon nanowires. However, it also improves the uncatalysed deposition of silicon across the substrate (Hofmann et al., 2003). It was expected, that with an increase in the uncatalysed deposition of silicon due to the introduction of a pulsed plasma, the diameter of the silicon nanowires would increase due to the deposition of amorphous silicon on the wire during growth. The wires would also be expected to taper due to the build up of amorphous silicon around the base of the wire while the wire was growing. However, this was not observed. This indicates that, with the growth times and conditions used, the uncatalysed deposition of amorphous silicon is very slight, not significantly adding to the nanowire diameter. The system used for this work deposits amorphous silicon thin films at an approximate rate of 0.3nm/s. For the deposition times used this would increase the average diameter of the nanowires by less than 6nm. This was not readily detectable on the SEM used.

The VLS mechanism can be invoked to explain the growth of the silicon nanowires in this work. One of the characteristics of the VLS mechanism is a gold tip on the end of the nanowires. Figure 6-4, showing both the SE and BSE images of the same nanowires, clearly shows the bright tip expected for nanowires grown by the VLS mechanism. Thus, the introduction of a modulated plasma has not affected the growth mechanism used to produce these silicon nanowires.
6.5 Conclusions

The use of PPECVD, with a silane plasma modulated at frequencies between 125Hz and 1000Hz, improved the density of silicon nanowires produced at low deposition temperatures. The average density of silicon nanowires increased with an increased plasma modulation frequency due to the repeated striking of the plasma. The proportion of the sample covered with silicon nanowires also improved with the use of high modulation frequencies. The average diameter of the silicon nanowires grown was found to be unchanged with increased plasma modulation frequency. Although the use of PPECVD tends to increase the deposition rate of amorphous silicon, for the deposition times used this did not affect the nanowire diameter. For low temperature growth of silicon nanowires the presence of a pulsed silane plasma improves the density and sample coverage of silicon nanowires. Due to these results the use of PPECVD is recommended as a worthwhile modification of PECVD to grow nanowires at low temperatures. The improvements in sample coverage and the uniform growth density across the substrate is beneficial for producing silicon nanowire based devices where the nanowires are to be used as a thin film. Due to this improved uniformity of growth, PPECVD will be used for the production of thin films of nanowires for device testing, as be will be discussed in Chapter 11.
7.1 Introduction
Gold is the most commonly used catalyst in the literature, as mentioned earlier. Gold is, however, an expensive material to use. Cheaper alternatives which produce similar densities of nanowires would be useful. The lower temperature limit on the growth of silicon nanowires is partly determined by the eutectic point of silicon and the catalyst. For the standard deposition conditions used in Chapter 6 the silicon nanowire growth could possibly be improved by using catalysts with lower eutectic points with silicon than gold.

The aim of the work described in this chapter was to try a variety of metal catalysts under the VLS mechanism using PECVD to improve the density of silicon nanowires under a given set of conditions. Due to technical limitations of the equipment used for this work the temperature could not be increased beyond ~345°C. For this reason the catalysts chosen had low melting points. The catalysts trialled were gold, tin, aluminium, indium, silver and copper. This work resulted in a series of SEM images, which are presented and an analysis of these is provided.

7.2 Experimental Details
Both glass and polished n-type Si(100) were used as substrates for the deposition of silicon nanowires in this study. The substrates were cleaned, as described in Chapter 4, before being transferred to a vacuum chamber for metal coating. No HF etch was performed on the crystalline silicon substrates leaving a native oxide layer intact to ensure non-epitaxial growth.

Catalyst layers with an average thickness of 100nm were deposited onto the substrates. The catalysts selected for this trial were chosen primarily for their relatively low melting points.
The purities of the catalysts were all high (Ag 99.9%, Al 99.97%, Au 99.99%, Sn 99.5%, Cu and In were laboratory reagent grade) and the metals themselves were cleaned in a propanol wash to remove surface material prior to evaporation. The shutter system was also used to block the first amount of metal evaporated from the filament to avoid contamination. The filament or tungsten boat was brought up to a temperature where the catalyst melted. Any volatiles in the, now liquid, metal evaporated first and were trapped on the shutter. The shutter was then subsequently opened to allow the pure metal to deposit onto the substrate.

After coating with the metal catalyst the substrates were transferred to the PECVD chamber for the growth of silicon nanowires. A series of the samples was produced using PECVD and a second series was produced using Pulsed PECVD which had been previously shown, in Chapter 6, to promote improved growth of silicon nanowires. The PECVD system used was of the parallel plate variety and used a RF signal to generate the plasma. The addition of square wave modulation of the RF signal provided Pulsed PECVD.

Once the samples were loaded into the chamber they were allowed to heat up to 335°C and outgas under an argon atmosphere of both 2.7 torr and 3.0 torr for 35 minutes. After this silane was introduced into the chamber and the samples were allowed to heat for a further 15 minutes before the plasma was struck. The change of gasses within the chamber tended to reduce the substrate temperature slightly and these 15 minutes allowed the temperature to return to 335°C. The deposition was performed under both 2.7 torr and 3.0 torr of silane and at a temperature of 335°C. Several different plasma powers and durations were used. The different plasma durations used ranged from 5 to 40 seconds for most catalysts. This deposition conditions are outlined in Table 7-1. A control sample using gold as a catalyst was present during each deposition.
Table 7-1: Deposition conditions for the different catalysts used in this study.

<table>
<thead>
<tr>
<th>Catalyst</th>
<th>Substrate Temperature (°C)</th>
<th>Chamber Pressure (torr)</th>
<th>Plasma Duration (s)</th>
<th>Plasma Power (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ag</td>
<td>335</td>
<td>2.7, 3.0</td>
<td>5,10,20,40</td>
<td>9</td>
</tr>
<tr>
<td>Al</td>
<td>335</td>
<td>2.7, 3.0</td>
<td>5,10,20,40</td>
<td>9, 10</td>
</tr>
<tr>
<td>Au</td>
<td>335</td>
<td>2.7, 3.0</td>
<td>5,10,20,40</td>
<td>9, 10</td>
</tr>
<tr>
<td>Cu</td>
<td>335</td>
<td>3.0</td>
<td>20,40</td>
<td>9</td>
</tr>
<tr>
<td>In</td>
<td>335</td>
<td>2.7, 3.0</td>
<td>5,40</td>
<td>10</td>
</tr>
<tr>
<td>Sn</td>
<td>335</td>
<td>2.7, 3.0</td>
<td>5,10,20,40</td>
<td>9, 10</td>
</tr>
</tbody>
</table>

The samples were left under the silane atmosphere for a further 10 minutes before the silane was removed and the system purged. The system was then allowed to cool to room temperature while being purged with argon. Once cooled, the samples were removed from the chamber and analysed using a Philips XL20 SEM or ZEISS 1555 VP FESEM.

7.3 Results

Each of the selected catalysts produced nanowires. However some catalysts, gold and tin, produced a high density of nanowires while the others grew only a few. The morphology of the nanowires and other nanostructures grown as part of this study was also found to be dependant on the catalyst that was used. A bright tip was present on the end of many of the nanowires; a visible high contrast tip or droplet like feature like this can be attributed to the presence of a metallic catalyst droplet. The contents of this droplet can be checked using a back scattered electron detector. Gold, and elements heavier than the silicon of which the nanowires consist, show up as bright regions under the BSE detector. The heavier elements back scatter more effectively leading to a brighter region. The nanowires grown at 2.7 torr were comparable to those grown at 3.0 torr.
Silver catalysed nanowires, such as shown in Figure 7-1, were found to have a range of diameters and lengths. These nanowires exhibited some growth defects such as kinking but tended to grow as long straight wires. Present on the end of some of the nanowires was a bright tip that was similar to the droplet seen on nanowires grown by the VLS mechanism. The visible nanowires were often found growing out of complicated structures such as in Figure 7-1. These are likely to have been catalysed and grown in the same process but consist of small nanowires and other indeterminate nanostructures. Not all of these structures produced nanowires.

Figure 7-1: Silver-catalysed silicon nanowires.
Aluminium was a largely unproductive catalyst yet it did produce some crystallite structures which, although nanowire-like in shape, were at a much larger scale having diameters significantly larger than nanowires grown by other catalysts. The diameters of the wire-like structures were fairly uniform. Many of the structures grown exhibited a droplet at one end, indicative of VLS growth. A single aluminium catalysed structure is shown in Figure 7-2. It should also be noted that these wire-like structures are pristine, growing without any of the more complicated structures in evidence, such as that for silver catalysts in Figure 7-1.

Figure 7-2: Aluminium-catalysed silicon wire-like structure.
Nanowires grown using gold as a catalyst are shown in Figure 7-3. As can be seen, the nanowires were grown at a high density. These nanowires are also of high aspect ratio and exhibit growth defects such as kinks.

*Figure 7-3: Silicon nanowires grown using gold as a catalyst.*
The nanowires grown using gold had largely uniform diameters, although some very fine wires can be seen in a higher magnification image in Figure 7-4. These nanowires showed some growth defects such as kinking and commonly had a droplet visible on one end of the nanowire. Although the nanowires were mainly straight and of high aspect ratio, some curled or worm-like structures had also been observed. The nanowires grown using gold as a catalyst have a much higher growth density (NW/µm$^2$) than other catalysts.

Figure 7-4: Gold-catalysed silicon nanowires showing a droplet on the tip and fine nanowires.
The use of copper as a catalyst yielded very few nanowires under the growth conditions used. Copper mainly produced a series of droplet-like structures on the surface of the substrate. Scattered amongst these were the occasional nanowire. A micrograph depicting this situation is shown in Figure 7-5. Copper nucleated nanowires had a largely uniform diameter and exhibited few growth defects. The density of growth of copper-nucleated nanowires was particularly low.

Figure 7-5: Copper-catalysed silicon nanowires and droplet-like structures.
Indium as a catalyst produced very few nanowires under the growth conditions used. Nanowires grown using indium as a catalyst are shown in Figure 7-6. These nanowires had a range of diameters as can be seen in Figure 7-6. The nanowires had both crystalline-like growth defects and amorphous worm-like structures, often within the same nanowire. A bright tip was visible on the end of a number of the nanowires.

Figure 7-6: Indium-catalysed silicon nanowires.
Tin produced nanowires at a high density as can be seen in Figure 7-7 and Figure 7-8. Tin-catalysed nanowires had two very distinct morphologies. The first is shown in Figure 7-7 and had a high density of very fine, uniform and long nanowires. These nanowires had few growth defects and tended to bend rather than kink.

![Figure 7-7: Long silicon nanowires grown using tin as a catalyst.](image-url)
The second morphology, shown in Figure 7-8, had a knotted appearance and appeared to be much more amorphous in structure. The second or knotted morphology tended to occur at higher silane partial pressures. However there is no clear cut line above which this morphology replaces the longer variant with both morphologies often present in different locations of the same sample. The curves and smooth changes in direction present in these structures may denote amorphous structures rather than the crystalline structures denoted by abrupt changes in growth direction as shown by the gold-catalysed nanowires. Alternatively the curves of the nanowires can be explained by a high density of defects such as stacking faults and twins (Wang et al., 1998).
The average diameter of the nanowires for the range of catalysts is shown in Figure 7-9. It can be seen from this figure that aluminium-catalysed wires had the greatest diameter, tin nanowires had the smallest and the other catalysts had very similar diameters under the deposition conditions used.

![Figure 7-9: Average silicon nanowire diameter for various catalysts averaged over the samples produced.](image)
To compare how well the nanowires catalysed by the different catalysts grew, the ‘coverage’ has been plotted in Figure 7-10. The coverage is a measurement expressed as a percentage of the sample covered by the nanowires as described in section 4.3.2. It can be seen in Figure 7-10 that gold produced the greatest coverage of nanowires at 84.5% followed by tin at 72.3%. The other catalysts had coverages below 12% indicating that tin and gold produce a much greater density of silicon nanowires for the growth conditions used. For the creation of films of nanowires to be used in devices, only gold and tin are suitable as they provide an even coating of small diameter nanowires.
To compare the growth of silicon nanowires by catalysed gold and by tin, a series of samples were produced using both catalysts on the one substrate. The catalysts were deposited via shadow masking to control the position of the films. As can be seen from Figure 7-11 the thickness of the films, the length of the wires and the overall morphologies are markedly different. The gold-catalysed nanowires grew in a much thicker film than the tin-catalysed nanowires. This can be seen by the relative height difference in Figure 7-11.

Figure 7-11: Gold-catalysed silicon nanowires (bottom of micrograph) and tin-catalysed nanowires (top of micrograph).
7.4 Discussion
The physical properties of the catalyst used to grow the silicon nanowires are likely to have an impact on the growth and morphology of the silicon nanowires. For example the melting point, or eutectic point of the catalyst and silicon determines the minimum temperature required for the growth of silicon nanowires via the VLS mechanism. This was mentioned in Chapter 5 where it was noted that nanowire growth did not occur for temperatures significantly lower than the bulk eutectic point. For reference, the melting points and eutectic points of the various catalysts are listed in Table 7-2.

<table>
<thead>
<tr>
<th>Catalyst</th>
<th>Melting Point °C</th>
<th>Si Eutectic Point °C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ag</td>
<td>961.78</td>
<td>845</td>
</tr>
<tr>
<td>Al</td>
<td>660.32</td>
<td>577</td>
</tr>
<tr>
<td>Au</td>
<td>1064.18</td>
<td>363</td>
</tr>
<tr>
<td>Cu</td>
<td>1084.62</td>
<td>802</td>
</tr>
<tr>
<td>In</td>
<td>156.6</td>
<td>156.63</td>
</tr>
<tr>
<td>Sn</td>
<td>231.93</td>
<td>231.9</td>
</tr>
</tbody>
</table>

*Table 7-2: Melting points and Si eutectic points of catalysts used for producing silicon nanowires (Wang et al., 2006, Hofmann et al., 2003, Lide, 2005, Massalski et al., 1986).*

From Figure 7-10 it was shown that gold and tin were the more effective catalysts for the growth of silicon nanowires under the growth conditions used. These two catalysts produced nanowires with a coverage seven to eight times greater than the other catalysts.

The growth of nanowires using gold as a catalyst and CVD is known to be via the VLS mechanism (Wagner and Ellis, 1964) if the growth temperature is high enough for growth to occur. The nanowires grown as part of this study have also shown the droplet like tip on the nanowires that is indicative of the VLS growth mechanism. Clearly defined catalyst droplets can be seen in Figure 7-4. This confirms that the VLS mechanism applies to the growth of silicon nanowires using PPECVD with a modulation frequency of 1000Hz. The coverage of
the sample by Au-catalysed nanowires was the highest of the catalysts trialled. Thus gold is an effective catalyst under the growth conditions used.

Wagner and Ellis (1964) also found that similar silicon whiskers or filaments could be grown using silver and copper via the VLS mechanism if the growth temperature was sufficiently high enough for growth to occur. It was found in this study that the use of both silver and copper as catalysts produced silicon nanowires although at a low density and coverage. The silver-catalysed nanowires often showed a bright tip under examination by the SEM which indicated the VLS mechanism or similar tip-driven mechanism is responsible for the growth. Droplet-like tips can be seen in the silver-catalysed nanowires in Figure 7-1. The copper-catalysed nanowires did not show any droplets on the end of the nanowires. This is the consequence of either the catalyst being consumed by the silicon nanowire to the point where the diameter and composition of the tip is indeterminate from the bulk, or a growth mechanism different to the VLS mechanism. The filaments produced by Wagner and Ellis (1964) were grown at a substrate temperature of 950°C which was significantly higher than the ~335°C used in this work. The difference between the eutectic points of Au-Si (363°C), Cu-Si (802°C) and Ag-Si (845°C) provides an explanation as to why the growth of nanowires, in this study, using these later catalysts was so ineffective, as shown by the coverage in Figure 7-10. The growth temperature used was a far below the eutectic point of silicon with copper or silver. Any resultant growth was sporadic and likely to be due to an alternate vapour-solid-solid growth mechanism.

 Aluminium has been used to produce epitaxially grown silicon nanowires of a 35nm diameter using a Vapour Solid Solid (VSS) mechanism (Wang et al., 2006). Their nanowires were grown at a temperature of 465°C after pre-annealing at 580°C and had a solid particle at the top of the nanowire. The wire-like structures observed in this study were likely to have grown through a similar mechanism as the growth temperature was far below the eutectic point,
needed for VLS growth. The crystallites grown in this study although of a much larger
diameter also had a particle present at the tip and did not show any preferred orientation.
The difficulty of growth in this situation is due primarily to the low temperatures used.

 Powdered tin as a catalyst has been used, in other studies, to produce silica nanowires via an
extended VLS mechanism (Sun et al., 2003). The silica nanowires grown using powdered tin
had a diameter of 100 to 200 nm and exhibited some interesting morphologies, branching
multiple times to produce ‘jellyfish’ like structures (Sun et al., 2003). In the present study a
thin film of tin was deposited onto the substrate rather than a powdered catalyst for the
growth of silicon nanowires rather than silica nanowires. The VLS growth mechanism is the
most probable explanation for these nanowires as the growth temperature was above the
melting point of tin. The diameters of the nanowires produced in this study were on average
54 nm as shown in Figure 7-9.

There were two distinctly different morphologies observed in the tin-catalysed nanowires
produced in this study. The first morphology had longer nanowires that curved gently and
were loosely bound (Figure 7-7). The second morphology consisted of a much more
convoluted crop of nanowires that twisted to a greater extent (Figure 7-8). This second
morphology is more likely to be amorphous in structure or consist of a large density of
growth defects but this has not been confirmed.

The difference in morphologies between the gold and tin-catalysed nanowires can be seen in
Figure 7-11. The more crystalline and larger diameter nanowires on the bottom of the image
are gold-catalysed. The fine material on the top of the image is tin-catalysed. Tin was an
effective catalyst, producing the thinnest nanowires and with a coverage second to that of
gold. However, tin far exceeded the coverage of the other catalysts under these deposition
conditions.
7.5 Conclusions

Silicon nanowires have been grown using silver, aluminium, gold, copper, indium and tin catalysts by PPECVD. It was found that gold and tin are the most effective catalysts at growth temperatures of approximately 335°C and chamber pressures of both 2.7 torr and 3.0 torr. The melting point and eutectic point of Au and Sn catalysts are close to, or less than, the deposition temperature used resulting in high density growth via the VLS mechanism. Tin was found to produce nanowires with an average diameter less than that of the other catalysts. The tin-catalysed nanowires showed two different morphologies, one of which appeared more amorphous than the other. Therefore for high density growth of silicon nanowires at ~335°C via pulsed PECVD tin and gold are the preferred catalysts.

Two catalysts can be used to fabricate silicon nanowire based photovoltaic devices. Gold and tin both produced high coverages of silicon nanowires. However, they produce two distinctly different morphologies. Both of these catalysts, and morphologies, can be used to produce photovoltaic devices. The devices produced form the two catalysts can then be compared to determine if the catalyst, or the morphology, influences the device characteristics.
CHAPTER 8: SILICON NANOWIRE GROWTH ON DIFFERENT SUBSTRATES

8.1 Introduction
To produce a photoconductive or photovoltaic device from films of silicon nanowires a method needs to be used to get light onto the device. Electrical contacts to thin film devices are usually made from both sides of the thin film. If an opaque substrate is used then the surface of the nanowire film must be coated with a Transparent Conducting Oxide (TCO). Alternatively, if a transparent conductive substrate can be used, a metal layer can be used for the top contact. Conventional thin film photovoltaic devices are often fabricated on transparent, ITO coated, substrates. To produce silicon nanowire thin film devices that are compatible with existing fabrication techniques it was necessary to investigate whether the nanowires could grow on transparent or Indium Tin Oxide (ITO) coated substrates. More complex device structures could be fabricated if the nanowires could be grown on layers of amorphous silicon. For example, a p-i-n junction formed from an a-Si:H p-layer and i-layer with n-type silicon nanowires. To this end this work also investigates whether silicon nanowires can be grown on thick layers (~300nm) of amorphous silicon.

The substrate upon which silicon nanowires are grown is known to affect the morphology of the silicon nanowires. The use of appropriately oriented substrates encourages the epitaxial growth of silicon nanowires (Wu et al., 2002). The use of epitaxial growth allows the production of vertically aligned nanowires, grown perpendicular to the substrate.

In this work a series of materials were trialled as substrates for the growth of silicon nanowires using PPECVD and a gold catalyst via the VLS mechanism. The substrates used were polished c-Si(110), c-Si(100), c-Si(111), polished stainless steel, polished copper (poly-
crystalline), microscope slides (borosilicate glass), Corning 7059 aluminosilicate glass, Corning ITO (Corning 7059 coated in ITO), Asahi ITO, microscope slides coated in amorphous silicon (a-Si:H) and amorphous silicon coated Corning ITO. Scanning electron microscopy was used to compare the growth of silicon nanowires on each of these substrates.

8.2 Experimental Details
Gold layers of average thicknesses of 100nm were deposited onto the various substrates to act as a catalyst for silicon nanowire growth.

All substrates were cleaned by the procedure outlined in Chapter 4. Following this, some of the crystalline silicon substrates were subjected to a 1 minute etch in 10% HF to remove the native oxide layer before being transferred into a vacuum system for deposition of the gold catalyst layer. Some crystalline silicon substrates were not given this etch prior to gold coating in order to preserve the native oxide layer. In addition, some crystalline silicon substrates previously treated with HF and coated with gold were given a second 30 seconds HF etch immediately prior to being placed in the chamber for the deposition of silicon nanowires.

Glass and ITO substrates were cleaned using decon-90 and ultra-pure water as described for the c-Si substrates. Copper and stainless steel substrates were polished to a mirror-like finish using increasingly fine grades of abrasives before being cleaned similarly to the glass and ITO substrates. The glass and ITO substrates to be coated with amorphous silicon were cleaned as above and were then placed in the PECVD chamber for the deposition of an approximately 300nm thick intrinsic amorphous silicon layer before coating with the catalyst layer. The thickness of the substrates is shown in Table 8-1.
Table 8-1: Thickness of materials used as substrates for the growth of silicon nanowires.

<table>
<thead>
<tr>
<th>Substrate</th>
<th>Thickness (mm) ± 0.05</th>
</tr>
</thead>
<tbody>
<tr>
<td>c-Si(110)</td>
<td>0.4</td>
</tr>
<tr>
<td>c-Si(100)</td>
<td>0.3</td>
</tr>
<tr>
<td>c-Si(111)</td>
<td>0.3</td>
</tr>
<tr>
<td>Stainless Steel</td>
<td>0.5</td>
</tr>
<tr>
<td>Microscope Slide</td>
<td>1.0</td>
</tr>
<tr>
<td>Corning Glass</td>
<td>1.1</td>
</tr>
<tr>
<td>Asahi ITO</td>
<td>1.1</td>
</tr>
<tr>
<td>Corning ITO</td>
<td>1.1</td>
</tr>
<tr>
<td>Copper</td>
<td>0.7</td>
</tr>
<tr>
<td>a-Si:H on microscope slide</td>
<td>1.0</td>
</tr>
<tr>
<td>a-Si:H on Corning ITO (~300nm &amp; ~500nm)</td>
<td>1.1</td>
</tr>
</tbody>
</table>

After coating with the metal catalyst and subsequent HF dip if required, the substrates were transferred to the PECVD chamber for the growth of silicon nanowires. Once the samples were loaded into the chamber they were allowed to heat up and outgas in an argon atmosphere of 3.0 torr for 35 mins. After this, silane was introduced into the chamber and the samples were heated for a further 15 minutes before the plasma was struck. The deposition was performed under 3.0 torr of silane and at a temperature of ~340°C. The plasma durations used were 10s, 20s, 40s and 60s. Plasma powers were maintained at approximately 9W. The plasma used for the work described in this chapter was pulsed with a 1000 Hz square-wave with a mark space ratio of 1:1 as described in Chapter 6. A control sample using a c-Si(100) substrate with an intact native oxide layer was present during each deposition. The samples were left under the silane atmosphere for a further 10 minutes following deposition before being allowed to cool to room temperature. The PECVD chamber was purged with argon during this process. Once cooled the samples were removed from the chamber and analysed using a Philips XL20 SEM and some were given further analysis on a ZEISS 1555.
Chapter 8: Silicon Nanowire Growth on Different Substrates

VP FESEM. The orientation of individual silicon nanowires was not conducted as part of this work.

8.3 Results

Although nanowires were grown using similar conditions on all of the substrates trialled, it was found that the relative density (NW/μm²) of the nanowires varied with the type of substrate used. The average density of nanowire growth on each of the substrates is illustrated in Figure 8-1 where the density is expressed in nanowires per square micrometre.

![Figure 8-1: Average nanowire densities on the substrates trialled.](image)
Chapter 8: Silicon Nanowire Growth on Different Substrates

The silicon nanowires grown on the crystalline silicon substrates had similar growth characteristics, in that the densities were similar on each crystalline orientation. No clearly aligned or epitaxial growth was observed on any of the crystalline samples regardless of pre-gold HF etch or post gold HF etch.

A sample of the nanowires produced on the c-Si(111) substrate is shown in Figure 8-2. As can be seen the nanowires are protruding from the substrate but did not otherwise showing any preferred orientation or alignment.

The high aspect ratio of the nanowires can also be observed in Figure 8-2. The nanowires grown on crystalline silicon substrates were generally long, straight and exhibited growth defects such as kinking. Similar results were observed for the other orientations of crystalline silicon.

Figure 8-2: Nanowire growth on c-Si(111) substrate (45° tilt).
Nanowires grown on the stainless steel substrate were, for the majority of samples, few and far between and exhibited a distinctly different morphology to other nanowires grown in this work. The morphology of these nanowire structures and the underlying substrate can be seen in Figure 8-3. These nanowires tended to coil and loop as opposed to the usual straight nanowires that exhibit growth defects.

Figure 8-3: Coiled nanowires on stainless steel substrates (45° tilt).
However, some regions of some samples had growths of ultra high density silicon nanowires of a more usual morphology as shown in Figure 8-4. The samples produced on stainless steel substrates showed no indication of alignment of the nanowires.

Figure 8-4: Ultra dense nanowires on stainless steel substrates.
Chapter 8: Silicon Nanowire Growth on Different Substrates

The copper substrates appeared to react fairly strongly with the amorphous silicon film that is deposited as a by-product during the growth phase of the silicon nanowires. Many platelet like structures were formed on the substrate leaving a black powdery finish on the surface of the copper. These platelets can be seen in Figure 8-5.

Figure 8-5: Platelet like structures grown on copper substrates.
Very few of the samples produced showed any indication of nanowire growth. However, on some samples in regions towards the outer edge of the area covered by the amorphous silicon film, nanowires did grow (Figure 8-6). In the regions where growth occurred the nanowires were produced with fairly high density and exhibited few growth defects, such as kinking, although some were observed. The nanowires produced on the copper substrates as shown in Figure 8-6 demonstrate a certain alignment and have grown vertically from the substrate in some regions. Figure 8-6 shows nanowire growth between areas of platelet-like growth.

Figure 8-6: Nanowires and platelets on a copper substrate (45° tilt)
Chapter 8: Silicon Nanowire Growth on Different Substrates

Figure 8-7 shows a micrograph from the FESEM providing greater detail of the morphology of the nanowires. It can be observed in Figure 8-7 that some nanowires have a droplet like tip, indicative of tip driven growth mechanism such as the VLS mechanism. Figure 8-7 also shows the nanowires as having grown in a cross-thatch arrangement. The nanowires have grown in mutually perpendicular directions. This is possibly due to epitaxial growth from crystallites within the substrate or the platelets themselves.

Figure 8-7: Silicon nanowires on a copper substrate (FESEM).

It was found that the density of nanowires grown on microscope slides was less than those grown on Corning glass. However the same nanowire morphology was produced on both types of substrate, consisting of long straight nanowires interspersed with gold agglomerate.
The nanowires grown on ITO-coated glass yielded the highest density of all the substrates measured. The density of nanowires grown on Corning ITO was greater than that produced on the Asahi ITO. Other than protruding from the substrate, no alignment of the nanowires was observed. An example of the high density nanowire growth produced on Corning ITO is shown in Figure 8-8 below.

Figure 8-8: High density nanowires produced directly on Corning ITO (45° tilt).
Some microscope slides and Corning ITO were coated with ~300nm of intrinsic amorphous silicon prior to the deposition of the gold layer. The density of nanowires produced on this material was significantly less than on the uncoated substrates. However, the morphology was similar with slightly more dendritic material than on the uncoated substrates. A micrograph of nanowires produced on amorphous silicon coated ITO is shown in Figure 8-9. No nanowires were observed to grow on a substrate coated with a thicker amorphous silicon layer (~500nm).

![Figure 8-9: Nanowires grown on a-Si:H coated ITO (~300nm).](image)

**Figure 8-9: Nanowires grown on a-Si:H coated ITO (~300nm).**
Chapter 8: Silicon Nanowire Growth on Different Substrates

The average diameter of the silicon nanowires was measured for each of the substrates as shown in Figure 8-10. The nanowire diameter was similar for each of the substrates, averaging 150nm.

![Figure 8-10: Average diameter for nanowires grown on each of the substrates.](image)

Figure 8-10: Average diameter for nanowires grown on each of the substrates.
8.4 Discussion

There are several factors that would influence the growth of silicon nanowires on various substrates. The temperature of the substrate directly influences the proportion of catalyst that is liquid on the surface, allowing the nanowires to grow via the VLS mechanism. The composition of the substrate determines if the nanowires can grow at all. If the substrate reacts with the catalyst, or amorphous silicon, the growth of nanowires can be stifled. Additionally, some growth mechanisms such as the SLS mechanism, use the substrate as a source of silicon (Xing et al., 2003). The VLS mechanism, using gold as a catalyst, at low temperatures requires a eutectic of gold and silicon to form. If it is in an available form, the substrate can be a source of silicon for this process.

The average diameter of the silicon nanowires grown during this work was 150nm on all of the samples, although some individual nanowires as large as 380nm and as small as 80nm were observed. The average diameter was largely unaffected by the change in substrate. This was to be expected as the diameter of silicon nanowires is known to depend primarily on the size of the catalyst droplet (Cui et al., 2001, McIlroy et al., 2004) and the silane partial pressure used during deposition (Westwater et al., 1997). There is no indication that the selection of the substrate would alter the average diameter of the silicon nanowires and this was what has been observed. This is significant as it indicates that the substrate a device is grown on can be changed from crystalline silicon to ITO coated glass without inadvertently changing the diameter of the silicon nanowires. As a result, the choice of substrate would not alter properties relating to diameter, such as the band-gap (Ma et al., 2003), which may need to be carefully selected for photovoltaic applications.

The nanowires grown on crystalline substrates in this work did not exhibit any significant evidence of aligned or epitaxial growth. This was regardless of the removal of the native oxide layer via a HF etch or the removal of the oxide over-layer on the gold as recommended
by Jagannathan, Nishi and co-workers (2006). They recommended a second HF etch immediately before the growth of silicon nanowires. For epitaxial growth, gold catalyst thicknesses such as 3nm (Jagannathan et al., 2006) are often used, or gold colloids with mean diameters of 20nm (Roest et al., 2006). These led to nanowires with diameters much smaller than the average 150nm produced in this work. Although producing a high density growth of silicon nanowires, the 100nm thick layer of gold used as a catalyst in this work may be too thick for reliable epitaxial growth to occur. Alternatively, the growth conditions may not be optimal for aligned growth at these low substrate temperatures, or the formation of an oxide layer after the HF etch and before the gold coating may be causing non-epitaxial growth. The catalyst layer thickness used in this work was larger than that in general used by groups trying to align silicon nanowires on crystalline silicon substrates (Jagannathan et al., 2006). However, this thicker catalyst layer was chosen as a standard as it produced dense films, or optimal growth, under the available deposition conditions. This dense growth was considered to be important for thin film silicon nanowire photovoltaics.

No alignment of the silicon nanowires was observed on glass substrates, ITO-coated glass substrates or amorphous silicon coated substrates. This was not unexpected as epitaxial growth requires a clean crystal surface to occur and these substrates were amorphous in nature. The surface of the stainless steel and copper substrates were polished and non-crystalline in nature. In addition, an oxide layer would have been present on the substrate before the deposition of the gold catalyst. As could be expected, stainless steel substrates did not show aligned growth. However, the copper substrate did demonstrate aligned growth in some regions although the dominant material was a platelet-like structure of unknown composition. The composition of these platelets was not explored. It has been previously noted by Phillips (1986) that copper substrates, when used with the deposition of amorphous silicon by CVD, produce a non-adherent black powdery layer similar to what was found in the work for this chapter. The ‘filamentaceous’ growth reported by Phillips was not dissimilar
from the view of low density platelets at low magnifications. The mutually perpendicular alignment of the nanowires could be due to epitaxial growth from the platelets or from crystallites within the substrate. The growth of silicon nanowires on this substrate is far from optimal given the extreme texturing that occurs upon deposition of the amorphous film by CVD during the preheat stage of the deposition but before the nanowire growth occurs. The nanowires on copper substrates only grew on a few of the samples investigated. This indicates that the growth, although possible, is marginal in the current system. The growth on the samples with nanowires could be a result of localised variations in the substrate, catalyst thickness or substrate temperature. Due to the low density of growth, these substrates are not likely to be of use for photovoltaic devices.

As stated above, the growth of silicon nanowires via the VLS mechanism is highly dependant upon temperature. The sample holder that attaches the glass materials to the heater block in the deposition is designed to loosely hold pieces of ITO and glass, therefore there is a gap of 0.1 to 0.2 mm between the surface of the ITO and the bottom of the heater block. The sample holder was designed for 1.1 and 0.5mm substrates. Other thickness substrates make poor thermal contact with the heater block. However, due to the pressures used, a significant amount of heat is transferred by conduction through the gas atmosphere. The holder for crystalline and metallic samples is radially further from the centre of the heater block and is thinner. This leaves the crystalline samples in loose contact and the metallic samples in firm contact with the heater block. As the microscope slides are thinner (0.1 mm) than the ITO coated materials and Corning glass, the slide would be in poorer thermal contact with the heater block and hence at a slightly lower temperature. Given that the deposition temperature being used is close to the eutectic point of gold and silicon, it can be argued that a slight decrease in temperature has a large impact on the quality of nanowire growth and thus the nanowire density. This is shown in Figure 8-1, where the density of nanowire growth on the microscope slides is less than that on the thicker glass-based materials. This argument also
applies for the amorphous silicon coated samples. The crystalline samples, being further from the centre of the heater block, could again be at a slightly lower temperature than the glass substrates resulting in a decreased nanowire density in comparison to the more optimally placed glass substrates.

From Figure 8-1 it can be seen that the conductive ITO coated materials, both Corning glass and Asahi ITO, produced nanowires at a higher density than the uncoated Corning glass of similar thickness. Previous work using PPECVD has indicated that part of the increase in density from using a 1000Hz pulsed plasma is the induced heating in the substrate (Parlevliet and Cornish, 2006). By introducing a conductive layer to the surface of the otherwise insulating glass substrate before the deposition of the gold catalyst layer, this effect could be enhanced. This results in a raised temperature and a higher density growth of silicon nanowires. By the same token, introducing a poorly conductive layer, such as amorphous silicon, between the ITO and gold layers appears to reduce this enhanced effect. This is shown by the poor densities of silicon nanowires on amorphous silicon coated substrates in Figure 8-1. The reduced growth densities on amorphous silicon can also be explained by the gold and silicon forming a eutectic without forming catalyst droplets as is the case on crystalline or glass substrates. This would occur where the gold became completely absorbed in the a-Si:H layer.

The presence and composition of the ITO coating on the glass may encourage the growth of silicon nanowires. The same glass substrate without ITO yielded poorer silicon nanowire growth. The disproportionation of the ITO at the growth temperature being used may allow free indium and tin to assist in the growth of the nanowires. The oxide itself may also encourage the growth of the silicon nanowires as oxides are known to assist the growth of silicon nanowires (Pan et al., 2005a). It was observed that the ITO from the two manufacturers used in this study produced nanowire thin films of different densities. The
may be variations in the composition of this ITO between manufacturers, although this was not explicitly measured. However, the composition of the ITO may be aiding the growth of the silicon nanowires.

8.5 Conclusions

The growth density of silicon nanowires was compared for a number of different substrates. Due to the thickness of the gold catalyst layer used, there was little evidence of aligned or epitaxial growth upon the crystalline silicon substrates despite HF etching. Copper and stainless steel substrates were found to be unsuitable substrates for the growth of silicon nanowires at the deposition temperature used, with only a few nanowires being observed. The composition of the curled nanowire like-growths on the stainless steel substrates was not investigated further as the density of growth was significantly lower than ITO or crystalline silicon substrates. This substrate was deemed unsuitable for the growth of silicon nanowires for photovoltaic applications. The only aligned growth observed was on the polished copper substrates.

Of the glass-based substrates, it was found that the thickness of the substrate had an affect on the density of nanowire growth; this being directly linked to proximity to the heater block. Both plain and ITO-coated Corning glass was used. It was found that nanowires grew with higher density on the ITO-coated substrates. It was proposed that the reason for this was the presence and composition of a transparent conducting oxide layer, the ITO, immediately preceding the gold catalyst layer. For samples where a poorly conducting amorphous silicon layer was interposed between the ITO and gold layers, poorer growth resulted.

Of all the substrates trialled, ITO-coated aluminosilicate glass was found to the most effective substrate to produce nanowires. This indicates that photovoltaic devices can be produced from silicon nanowires in a procedure compatible with existing fabrication
techniques and device designs. The low growth density of silicon nanowires on amorphous silicon indicates that in nanowire-amorphous silicon hybrid devices, the nanowires should be most easily grown as part of the p-layer or i-layer. The ease of growth of silicon nanowires on transparent substrates has many industrial applications where silicon nanowires need to be grown on a transparent conductive substrate, such as solar cells and photodetectors.
CHAPTER 9: FURTHER STUDIES USING PPECVD

9.1 Introduction
Silicon materials need to be doped to create the p-type and n-type materials used in such devices as thin film solar cells. As mentioned in Chapter 8, silicon nanowires did not grow at high density on thick layers of amorphous silicon. This indicates that they should be used as either p-type, n-type or left intrinsic. To create the p-type or n-type silicon nanowires through \textit{in situ} doping the growth of the nanowire needs to be conducted in a mixture of silane and diborane or phosphine. The silane gas used was undiluted whereas the diborane and phosphine were both 1% in argon. For the same dopant ratios used for creating the standard amorphous silicon devices, the partial pressure of silane in a chamber at a total pressure of 3.0 torr would need to be less than 0.6 torr. The aim of the work described in this chapter was to determine if silicon nanowires would grow at this partial pressure under the standard growth conditions described in previous chapters. Several other parameters such as plasma duration have also been explored.

The work described in this chapter aims to determine the affect of a range of different deposition conditions, on the growth and morphology of silicon nanowires grown using PPECVD via the VLS mechanism. The parameters to be explored are the silane partial pressure, gas flow rate, PPECVD plasma duration and the duration of CVD after the PPECVD duration (post-PPECVD CVD).

9.2 Experimental Details
Several different parameters were explored to determine their effect on the growth of silicon nanowires by PPECVD. To do this a series of samples was produced using a common base recipe. With each series of samples only one variable changed at a time with all the other variables held constant.
ITO-coated aluminosilicate glass substrates were used for all samples. These substrates were cleaned as per the procedure in Chapter 4 before being transferred into a vacuum system for deposition of the catalyst layer.

A gold catalyst was used for the growth of nanowires on the majority of samples. In a separate series of samples, a tin catalyst was also used to determine the affect of silane partial pressure and flow rate upon the growth of nanowires grown using this catalyst. Catalyst layers of 100nm thickness were deposited onto the substrates by thermal evaporation of gold wire (99.99%) or tin foil from a tungsten wire under vacuum. Gold was used as it is the preferred catalyst to grow silicon nanowires since the eutectic temperature of gold and silicon is a relatively low 363°C. Tin was also examined as it has been previously shown to produce high density nanowires of a different morphology compared to gold nucleated nanowires (Parlevliet and Cornish, 2007).

The catalyst-coated samples were loaded into the PECVD chamber and mounted on the heater block. The samples were heated to 335°C for 35 minutes in the presence of 3.0 torr of argon. The argon was then removed and silane, or a mixture of silane and argon at 3.0 torr, was introduced into the chamber. The system was allowed to stabilise for a further 35 minutes before the deposition commenced. Samples were produced using different silane partial pressures, between 1.05 torr and 3.0 torr, in several increments. Several gas flow rates were trialled at each of the partial pressures used.

A square wave generated by a pulse generator (SRS Model DG535) modulated the 13.56MHz signal used to generate the plasma. A modulation frequency of 1000Hz was used and the mark space ratio was held at a constant ratio of 1:1. Plasma duration was kept at a constant 40 seconds for the partial pressure and flow rate samples. The gas flow and substrate temperature were maintained for a further 10 minutes of post PPECVD CVD
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time. Other samples were produced using PPECVD times of between 0 and 120 seconds
with a subsequent 10 minutes of post-PPECVD CVD. Further samples were produced using
a fixed 40 seconds of PPECVD time with a post PPECVD CVD range from 0 and 30
minutes. After the deposition the system was purged with argon and cooled to near room
temperature, the samples were removed and mounted on SEM stubs for measurement. The
samples were analysed using a Phillips XL20 SEM at Murdoch University.

9.3 Results
Silicon nanowires of high density were successfully grown using different growth conditions.
Many of the nanowires exhibited growth defects. A micrograph of the high density silicon
nanowires grown, exhibiting numerous growth defects such as kinks, is shown below in
Figure 9-1.

![Figure 9-1: High density growths of silicon nanowires that were exhibiting growth defects.](image)
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The change in coverage of the nanowires by varying the silane partial pressure was measured from the electron micrographs. Coverage is a measurement that relates to the diameter, density and length of the nanowires and describes how much of the sample is covered by the nanowires as described in section 4.3.2. Figure 9-2 shows, that for higher silane partial pressures (3.0 torr), the coverage of nanowires grown with a gold catalyst for all flow-rates approached a similar level. For lower partial pressures the nanowire coverage decreased rapidly below 1.5 torr, or 2 torr for low gas flow rates. The legends in the following figures (Figure 9-2, Figure 9-3, Figure 9-4 and Figure 9-5) refer to the flow rate of silane as set on the PECVD system. The flow rate is expressed in standard cubic centimetres per minute (sccm).

![Figure 9-2: Nanowire coverage where silane partial pressure is varied for different silane flow rates using a gold catalyst.](image-url)
Similar trends were observed for nanowires produced using tin as a catalyst. Figure 9-3 shows the trend in which the tin-nucleated nanowires have a greater coverage for higher silane partial pressures. There were no nanowires observed to grow below approximately 1.5 torr.

![Figure 9-3: Nanowire coverage for different silane partial pressures and for different silane flow rates with a tin catalyst.](image)
Chapter 9: Further Studies Using PPECVD

The diameters of the nanowires grown with gold catalysts were also measured for the same range of pressures and flow-rates used above. As can be seen in Figure 9-4, the average nanowire diameter did not vary with silane partial pressure. The nanowire diameter also did not vary significantly with the silane flow rate, within the specified error bounds.

Figure 9-4: Average nanowire diameter for different silane partial pressures and flow rates using a gold catalyst.
Nanowires often exhibit growth defects such as kinks. The number of kinks/cm$^2$ has been measured for the range of silane partial pressures and flow rates mentioned above for gold-catalysed nanowires. The number of kinks in the nanowires was found to decrease for higher silane partial pressures as shown below in Figure 9-5. The number of kinks also tends to decrease below 1.5 torr which was due to the decreasing nanowire coverage below this point. Where there were fewer nanowires, the overall number of kinks in the sample was reduced as there were fewer nanowires to exhibit growth defects. The nanowires exhibit a greater density of growth defects for lower silane partial pressures when the decrease in coverage for lower partial pressures is taken into account.

![Figure 9-5: The average number of kinks per cm$^2$ for gold-catalysed silicon nanowires produced at different silane partial pressures.](image)
Nanowires were produced using a range of different PPECVD plasma durations with a fixed post PPECVD CVD time of 10 minutes. It was found that there was a distinct increase in nanowire coverage of 35% when a pulsed plasma, of even 5 seconds duration was introduced. For pulsed plasma durations of greater than 5 seconds a nearly linear increase in coverage was observed as shown in Figure 9-6.

![Figure 9-6: Silicon nanowire coverage versus plasma duration for gold catalysts. The plasma power was approximately 30W for all samples, the deposition temperature was 335°C and the flow rate of silane was 194 sccm at a partial pressure of 2.5 torr.](image)

Figure 9-6: Silicon nanowire coverage versus plasma duration for gold catalysts. The plasma power was approximately 30W for all samples, the deposition temperature was 335°C and the flow rate of silane was 194 sccm at a partial pressure of 2.5 torr.
Samples were produced where the post-PPECVD CVD time was varied while the PPECVD plasma time was held constant at 40 seconds. Increasing the post-PPECVD CVD time was found to slightly increase the nanowire coverage from 89% to 96%. This can be seen below in Figure 9-7.

![Figure 9-7: The coverage of nanowires improves slightly for greater post PPECVD CVD durations when a gold catalyst is used.](image)
The diameter of nanowires produced with varying PPECVD plasma durations was also measured and found to be constant, within the estimated error margin, for all plasma durations. However it was noted that there was an increase in diameter in comparison to CVD-only growth. This can be seen in Figure 9-8.

![Figure 9-8: Average nanowire diameters for different PPECVD durations for gold catalysts.](image_url)
The diameter was also measured for nanowires grown with a constant PPECVD duration and different post PPECVD CVD times. As shown in Figure 9-9, it was found that the average diameter of the nanowires was not affected by altering post-PPECVD CVD durations.

![Figure 9-9: Average nanowire diameters for different post PPECVD CVD durations.](image)

### 9.4 Discussion

Silicon nanowires were found to show decreased coverage for lower silane partial pressures when grown by PPECVD. This was consistent for all flow rates and both the gold and tin catalysts. However, the decrease was more pronounced for lower silane flow rates. A proposed reason for this decrease is that there is a limited amount of silane present and flowing through the chamber during the initial heating and growth times. To fully create a eutectic of gold and silicon, or tin and silicon, a certain amount of silicon needs to be present in the vapour phase. The amount of vapour phase silicon required would be dependant on
the sample size and the thickness of the catalyst layer. From this it can be reasoned that where there was a low flow of silane through the chamber, and an overall low partial pressure, the conditions were not favourable to high nanowire coverage as there was insufficient silicon. Presumably for high enough flow rates, the nanowire growth would occur for lower silane partial pressures as the amount of silicon the sample is exposed to would increase. This effect was observed for gold-catalysed nanowires as shown in Figure 9-2. One way around this poor growth of silicon nanowires would be to use thinner catalyst layers or fewer samples in each deposition to reduce the amount of gold present; although this has not been tested. Tin-catalysed nanowires did not show the same trends as strongly. However, the general trend towards a better growth at higher silane partial pressures was shown in Figure 9-3. Westwater, Gossain and co-workers (1997) found a similar trend in gold-catalysed silicon nanowire growth where the growth was denser at higher silane partial pressures. The pressure used in their work ranged from 0.01 torr to 1.0 torr of silane in a total chamber pressure of 10.0 torr as opposed to the 3.0 torr used in this work. They comment that when the silane pressure was increased the potential of the vapour was also increased leading to thinner wires at a higher growth density (Westwater et al., 1998). This was a catalyst layer effect; the droplet size was determined by the catalyst layer thickness and nanowire growth occurred where conditions were thermodynamically favourable (Westwater et al., 1998).

Hofmann, Ducati and co-workers (2003) found that nanowires grew at higher growth rates where a higher silane partial pressure was used. The increase in coverage for higher partial pressures shown in Figure 9-2 agrees with this, as coverage is a measurement relating density, diameter and length of the nanowires. By producing the nanowires at higher silane partial pressures the nanowire coverage should increase. However due to constraints with the deposition system this was not investigated. As stated earlier in Chapter 5, there is a link between the total chamber pressure and the temperature of the substrate. That is, at higher pressures the substrate tends to have a higher temperature due to improved transference of
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heat from the heater block to the substrate. This increased temperature of the substrate would also aid the growth of the silicon nanowires, increasing the coverage of the sample.

The results shown in Figure 9-4 indicate that there was no measurable (within error margin), change in the diameter of the gold-catalysed silicon nanowires over the range of pressures trialled. This was slightly contrary to the results of other groups such as Westwater, Gosain and Usui (1998) who found that the nanowire diameter decreased for higher silane pressures using CVD. Although it should be noted that the experimental range they used was greater than the 2.0 torr trialled here, a larger effect would be expected. However, Hofmann, Ducati and co-workers (2003) found that by using PECVD, there was little change in nanowire diameter over the pressure range of 0.3 torr to 1.8 torr. This was a similar partial pressure range to that used in this work. The findings in this current work reflected those of Hofmann, Ducati and co-workers (2003). The dominant variable impacting on nanowire diameter is the catalyst layer, specifically the catalyst droplet size (Cui et al., 2001, McIlroy et al., 2004). The droplet size is affected by the thickness of the catalyst layer. The catalyst layer thickness was left fixed at 100nm for this work so this should result in a constant nanowire diameter as was found. 100nm was used as consistent results have been achieved using this catalyst layer thickness.

The number of kinks in the nanowires grown in this study was measured. The number was found to decrease for higher silane partial pressures as shown in Figure 9-5. There was also a decrease in the number of kinks for low partial pressures. The reduction in the number of kinks for lower partial pressures can be explained by the lower nanowire coverage for these pressures. With this taken into account, a general trend emerges of a reduced number of kinks or straighter nanowires when a higher silane partial pressure was used. This result was a bit surprising as Westwater and co-workers (1998) found that higher total pressures and higher silane partial pressures (Westwater et al., 1997) produced nanowires with more growth.
defects (kinks). The kinking of the nanowires is believed to be associated with instabilities at the liquid/solid interface and is due to high growth rates (Westwater et al., 1997). As the nanowires tend to have a higher growth rate at higher silane partial pressures (Hofmann et al., 2003), the nanowires should have more of a tendency to kink. As this was not the result obtained, the high number of kinks for low silane partial pressures could be the result of local plasma instabilities in the PPECVD system used over the range of pressures tested (1-3 torr). Alternatively this variance with silane partial pressure may be the result of using pulsed PECVD.

Figure 9-6 demonstrates the abrupt increase in the coverage of silicon nanowires when a pulsed plasma is struck as opposed to straight CVD growth. It has previously been shown that the use of a gas plasma increased the density and growth rates of silicon nanowires (Hofmann et al., 2003, Colli et al., 2006) when used at similar conditions for CVD growth. In Chapter 9 it was demonstrated that the use of a pulsed plasma showed a similar enhancement of nanowire growth in comparison to conventional CVD growth even for very short plasma durations of 5 seconds. For longer plasma durations the nanowire coverage increased as was consistent for continued nanowire growth extending the length of the nanowire, but not to the same dramatic extent as the initial few seconds of pulsed plasma assisted growth which seems to aid in the nucleation of the nanowires. Figure 9-7 demonstrates that for a fixed duration of PPECVD, a period of post PPECVD CVD growth did increase the coverage of silicon nanowires. This was again consistent with continued nanowire growth by CVD. This indicates that when growing nanowires by PPECVD, the post-PPECVD CVD duration, although aiding the coverage of nanowires on the sample, is not necessary for the growth of high quality silicon nanowires.

It has previously been shown that the diameters of silicon nanowires increases when grown via PECVD as compared to CVD (Colli et al., 2006). This same trend was observed in Figure
where a noticeable jump in nanowire diameter occurred when a 5 second period of PPECVD was introduced. This was a result of the increased deposition rate of amorphous silicon via PPECVD causing the nanowires to become coated in a layer of amorphous silicon, resulting in an increased diameter. It was expected that the nanowires would show tapering when longer periods of PPECVD were used. This is because uncatalysed amorphous growth would be deposited on the sides of the nanowires as they grew with larger thicknesses at the base of the nanowire. This effect was seen for PECVD growth (Hofmann et al., 2003). However this was not observed within the error margins of the data collected in this work. Similarly, no noticeable increase in diameter of the nanowires due to longer post PPECVD CVD durations was observed. This indicates that the uncatalysed amorphous growth is not significant under the deposition conditions used.

9.5 Conclusions

Silicon nanowires were produced using a range of different growth parameters. By changing the partial pressure of silane in the chamber it was found that the silicon nanowires grew with a greater coverage for higher silane partial pressures. It was found that the diameter was not affected by the change in silane partial pressure. Extremely low coverage of silicon nanowires was found for low flow rates and for silane partial pressures nearing 1 torr for gold-catalysed silicon nanowires and below 2.0 torr for tin-catalysed nanowires. This indicates that in situ doping of the silicon nanowires to the level used in the standard a-Si:H recipe is not feasible under the growth conditions used. However, very slight doping of the silicon nanowires may be possible by using the diborane and phosphine dopant gasses at similar partial pressures at which argon was used in this chapter. The partial pressures used for doping amorphous silicon may not be the most appropriate for doping silicon nanowires, due to the difference in growth mechanisms between these materials. However, these partial pressures are a known starting point for good quality doped silicon on the deposition system being used and are a good starting point for doping. The nanowires were also found to exhibit a greater density of
growth defects for lower silane partial pressures when the decrease in coverage for lower partial pressures was taken into account.

The use of PPECVD has been shown to increase the coverage of nanowires when compared to conventional CVD for even very short plasma durations. The use of a period of post PPECVD CVD was found to improve the coverage of silicon nanowires only slightly. This indicated that high density silicon nanowires can be produced using only very short periods of PPECVD. This simplifies the production process.
10.1 Introduction
For many thin film a-Si:H photovoltaic devices, creating an electrical connection to the
device is done using aluminium contacts. Aluminium is commonly used as a back-contact to
the device and is deposited after the fabrication of the device itself. As such, it is useful to see
if aluminium will adhere to silicon nanowires when evaporated onto a thin film of nanowires.
It is also useful to investigate how aluminium coatings affect the morphology of silicon
nanowires when deposited as a thin film. Thin films of silicon nanowires may be used as part
of semiconductor devices such as solar cells. For many applications a degree of durability is
required. Therefore, the level to which silicon nanowire thin films can be damaged by
everyday ‘wear and tear’ is also of interest.

This work aims to determine what affect coating silicon nanowire films with varying
thicknesses of aluminium has on the morphology of the nanowires. Both tin-catalysed and
gold-catalysed silicon nanowires were used. This work also aims to observe how susceptible
to damage silicon nanowire thin films are either when pristine or coated in different thickness
layers of aluminium.

10.2 Experimental Details
ITO-coated aluminosilicate glass substrates were used for all samples. These substrates were
cleaned, by the procedure outlined in Chapter 4, before being transferred to a vacuum system
for deposition of the catalyst layer.

Gold and tin catalysts were used for the growth of silicon nanowires via the VLS mechanism.
Tin was used as it is also a good catalyst for the growth of high density, low diameter silicon
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Silicon nanowires were grown at high density using Pulsed PECVD. Silane was used as a source of silicon for VLS growth of the silicon nanowires. A square wave generated by a pulse generator (SRS Model DG535) was used to modulate the 13.56MHz signal used to generate the plasma. A modulation frequency of 1000Hz was used and the mark space ratio was held at a constant ratio of 1:1. After the deposition the system was purged with argon, cooled to near room temperature and the samples were removed for further treatment. A range of different deposition conditions were used and nanowire samples with a similar coverage were selected for further coating with aluminium.

After deposition the samples were coated in aluminium of different thicknesses. This was measured by a quartz crystal microbalance. A range of thicknesses up to 2µm were deposited. Each different layer thickness was deposited in a single deposition. The samples were mounted to a metal framework, inverted over a filament. The samples were not maintained at a constant temperature and may have heated up during the metal coating process. The samples were then subjected to various forms of damage including being scratched with a scalpel tip, scraped with a scalpel blade and abraded with both fine (SiC 4000) and coarse abrasives (Wet and Dry 400). The samples were then mounted on Scanning Electron Microscope (SEM) stubs for measurement. The samples were analysed using a Phillips XL20 SEM or ZEISS 1555 VP FESEM.
10.3 Results

The addition of a layer of aluminium to the silicon nanowires tended to increase the average diameter of the gold-catalysed nanowires. The average diameter is the diameter of the nanowire coated with aluminium. The nanowire diameter increased for larger aluminium layer thicknesses as the aluminium coated the nanowire to a larger degree. This trend can be seen in Figure 10-1 below.

![Figure 10-1: The increase in average nanowire diameter with aluminium layer thickness.](image)

The morphology of the nanowires changed with the addition of the aluminium layer for both gold and tin-catalysed silicon nanowires. For thin aluminium coatings there was little change in the overall morphology. This can be seen in the similarities between the pristine gold-catalysed nanowires in Figure 10-2a, the 97nm aluminium layer coated nanowires in Figure 10-2b and 140nm aluminium layer coated in Figure 10-2c. When the aluminium layer thickness is of the order of 500nm as in Figure 10-2d, there were noticeable accumulations of aluminium on some regions and a noticeable texturing of the nanowires themselves. For a
layer thickness of 1.3\(\mu\)m the morphology of the nanowires changed dramatically as can be seen in Figure 10-2e. The addition of this thickness of aluminium coated the silicon nanowires in a 'spiked' sheath. Where a thicker layer of aluminium was used such as 2\(\mu\)m in Figure 10-2f the spiked appearance was reduced as the individual crystal-like formations merged together.

Figure 10-2: Scanning electron micrographs of a) Pristine gold-catalysed silicon nanowires and silicon nanowires coated with aluminium to a thickness of b) 97nm, c) 140nm, d) 500nm, e) 1.3\(\mu\)m and f) 2\(\mu\)m.
Similar trends were observed with tin-catalysed nanowires as can be seen below in Figure 10-3. There was little or no change to the nanowire morphology for aluminium coating thicknesses of below 1.3µm. This can be seen in the similarities for the nanowire morphology in Figure 10-3a, b, c and d between the pristine nanowires (Figure 10-3a) and the coated nanowires. The nanowires in Figure 10-3d exhibited a similar spiked morphology to the gold-catalysed nanowires at the same thickness of aluminium.

Figure 10-3: Scanning electron micrographs of a) Pristine tin-catalysed silicon nanowires and silicon nanowires coated with b) 97nm, c) 140nm, d) 500nm and e) 1.3µm of aluminium.
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Through the durability tests it was observed that the silicon nanowires were very susceptible to being removed from the substrate with the contact of a scalpel, an abrasive or a gloved finger. The damage inflicted on the sample with varying materials is shown below in Figure 10-4. Figure 10-4a shows a trench cut into the nanowire film with the tip of a scalpel. In Figure 10-4b the edge of a region scratched with a scalpel blade can be seen; the demarcation between nanowire film and scraped region can be seen clearly.

In Figure 10-4c the region was only lightly scratched with a fine abrasive and no scratches are apparent. However, there was evidently some mechanical alignment of the silicon nanowires by the abrasive as seen by the predominant alignment across the micrograph. In contrast to the fine abrasive in Figure 10-4c, the coarse abrasive in Figure 10-4d has cut trenches and grooves into the nanowire film. Little mechanical alignment was observed for the coarse abrasive except where the nanowire film was only lightly scratched. It was found that the aluminium layer coating the nanowires did in no way protect the samples from being readily damaged regardless of the thickness of aluminium used.

Figure 10-4: Gold-catalysed nanowires damaged with a) a scalpel tip, b) a scalpel blade, c) a fine abrasive and d) a coarse abrasive.
Chapter 10: Aluminium Coating of Silicon Nanowires

Through the abrasion or scratching of the nanowire film, large collections of nanowires formed in tightly bound agglomerates. These formations can be seen in Figure 10-5 where a scalpel edge has scraped the nanowire film off the substrate. These formations tended to appear where the nanowires were mechanically removed from the substrate and were a result of the collection of many nanowires into large clusters. The nanowire agglomerates have a striking resemblance to felt and other fibrous material.

![Figure 10-5: A nanowire roll or agglomerate as result of the nanowire film being scraped off the substrate.](image)

It was also noted that the mechanical removal of the nanowires from the substrate tended to break the nanowires as well as forcibly removing the nanowires from the substrate. This effect can be seen in the cluster of nanowires in Figure 10-6. While some ends show a catalyst tip, other ends have an uneven appearance. Also seen in this micrograph is one
Chapter 10: Aluminium Coating of Silicon Nanowires

nanowire that has been truncated in comparison to the other nanowires; likely through multiple breakages.

Figure 10-6: Silicon nanowires removed from the substrate by mechanical means exhibiting breakages.

10.4 Discussion
Aluminium deposited by thermal evaporation was found to adhere to silicon nanowires. This was more noticeable for larger deposited layer thicknesses. However, Figure 10-1 did show an increase in the average diameter of the silicon nanowires. This increase in diameter can be attributed to the amount of aluminium adhering to the nanowire surface. The effect of the aluminium coating on the nanowire morphologies was similar for both the gold and tin catalysts that were used. The initial nanowire morphology did not appear to affect how the aluminium adhered to the nanowires. For the thin layers of aluminium on both gold and tin-catalysed nanowires, only very small differences in the overall morphology were observed as there was simply insufficient material to be readily visible under the SEM. For thicknesses
greater than 1.3µm, the aluminium coating was much more pronounced and readily visible. The coating was not as even as would be expected with the thermal evaporation of a metal from a source onto a flat substrate. The aluminium tended to agglomerate in crystal-like structures giving the nanowires an extremely textured ‘spiked’ appearance. The aluminium had completely covered most nanowires for thicknesses greater than 1.3µm. This even coating is important if contact to the entire nanowire is required. For greater thicknesses of aluminium the spiked appearance was less pronounced as the texturing was smoothed out by the large quantities of aluminium incident on the nanowire. The even coating of material all of the way around the nanowires for large aluminium thicknesses was unexpected. When coating material with aluminium via a thermal evaporation source on a macro scale, shadow masks produce a relatively sharp edge. However, the aluminium atoms have a certain amount of energy when leaving the tungsten filament. This energy may be enough for some mobility of the aluminium as it encounters the nanowire, allowing the even coating of the nanowire. This energy is also sufficient to allow crystal-like growth around the circumference of the nanowire, similar to the crystal formation from a liquid.

As was expected, subjecting the nanowire films to various forms of damage was found to easily remove the nanowires from the substrate. Coating the nanowires in films of aluminium did not provide any protection from damage. Where a scalpel tip was scratched along the substrate, deep trenches formed with the excess nanowires accumulating in bundles along the trench. Using a scalpel edge to scrape the nanowires off the substrate resulted in most of the nanowires being removed and piled up in fabric like agglomerations as in Figure 10-5. This is of interest in that it indicates when removing nanowires from a substrate via a scraping method, the nanowires need to be separated before they can be analysed by techniques such as TEM. This can readily be achieved through dispersion and dilution of the nanowires in a solution with the aid of ultra-sonication.
Abrading the nanowire films with a fine abrasive, or simply a gloved finger, tended to partly align the nanowires in regions where the nanowires were not removed from the substrate. This indicates that if it is desired, post deposition alignment of the silicon nanowires through mechanical means is possible if a fine abrasive or comb-like tool could be used. Coarse abrasives did not result in significant mechanical alignment of the silicon nanowires. Due to the larger grain size the nanowires were removed completely from the substrate rather than being aligned. The nanowires, when removed from the substrate through mechanical means, often exhibited breakages as shown in Figure 10-6, indicating that should nanowire devices be prepared in bulk on a substrate, a less damaging method of removal from the substrate should be used. These breakages would affect the commercial viability of an electronic device produced from silicon nanowires.

10.5 Conclusions
Aluminium readily adhered to silicon nanowires when thick layers of aluminium were used. This indicates that aluminium, particularly in relatively thick layers, can be used as the back-contact on a device incorporating silicon nanowires. Coating silicon nanowires in aluminium to create electrical contacts can significantly alter the morphology of the nanowires. For small thicknesses of aluminium this change is negligible. However, for large aluminium film thicknesses the nanowires exhibit a spiked profile where the aluminium has accumulated. This holds ramifications for creating electrical contacts with the nanowires in a bulk form. To provide a good contact to the entire nanowire an even coating of aluminium can be applied by using large thicknesses of aluminium. The nanowire films were found to be susceptible to mechanical deformation and easily removed from the glass substrate. Some mechanical alignment of the nanowires was found and this indicated that post deposition alignment of the nanowires can be readily achieved. Alternate applications such as creating a nanowire felt or thread may also be possible through mechanical means.
CHAPTER 11: SILICON NANOWIRE DEVICES

11.1 Introduction
The aims of this work were to produce devices using bulk intrinsic silicon nanowires and doped amorphous silicon layers. This ultimate aim could be achieved once the production process was investigated. The investigations of the previous chapters contributed to the goal of producing a silicon nanowire based photovoltaic device. By using the results in previous chapters high density silicon nanowires could be reliably grown on transparent ITO coated substrates. The nanowires and growth conditions in this work have aimed at producing high density films of nanowires rather than very small diameter nanowires. High density nanowires could be grown using two catalysts, tin and gold, which allowed the effect of different nanowire morphologies to be investigated. In Chapter 9 it was found that only very weak \textit{in situ} doping of the nanowires would be possible under the current growth conditions. Using these results, several different photovoltaic devices which incorporate silicon nanowires were designed and investigated. This chapter details the device designs and their properties.

There are several expected advantages of using silicon nanowires in photovoltaics. These advantages include a high absorbance of light as well as the ease and low cost of manufacture of thin film devices. By using small diameter nanowires, quantum confinement effects could be taken advantage of. However there are advantages, even with the larger diameter nanowires such as those produced in this work. For example, the thin film devices could show an improved resistance to photodegradation if crystalline silicon nanowires were used, due to their crystalline content.
Gold is widely used to produce crystalline silicon nanowires due to the low Au-Si eutectic point (363°C) (Wagner and Ellis, 1964). Tin has only recently been used as a catalyst in the fabrication of silicon nanowires by either a thermal method (Chen et al., 2007, Shao et al., 2005), hydrogen-radical assisted method (Jeon et al., 2009) or PPECVD, as shown in Chapter 7, although it had earlier been mentioned as a catalyst that may be suitable for low-temperature vapour liquid solid growth (Iacopi et al., 2007, Sunkara et al., 2001). The density at which nanowires have been produced by PPECVD makes them suitable for use as a thin film photovoltaic material. Tin is also a promising candidate for the production of semiconductor nanowire devices due not forming intermediate compounds with silicon, being electrically neutral in silicon and having limited silicon solubility (Iacopi et al., 2007). In comparison, gold is known to act as a recombination centre in silicon, adversely affecting the minority carrier lifetime (S.M. and K.K., 1981) and hence device performance of a photovoltaic device produced using silicon with gold impurities. Despite gold being a poor choice of catalysts for producing silicon nanowires for photovoltaic applications it was used in the devices created as part of a this project for a number of reasons. Gold is a preferred catalyst for nanowire growth and has been used by other groups, recently, to produce silicon nanowire photovoltaics (Kelzenberg et al., 2008, Tian et al., 2007), this makes comparison between the devices possible. In the context of the work in this project, the use of both gold and tin allows a comparison between nanowire devices created using both catalysts. This allows a range of diameters and morphologies to be tested within a hybrid thin-film amorphous silicon and nanowire device.

The devices created as part of this project, were a hybrid of thin-film amorphous silicon and highly textured silicon nanowire layers either as an intrinsic material or slightly p-type. The electrical characteristics of the created devices were measured using IV characterisation techniques. Some samples were also imaged using an FESEM to observe surface
morphism changes from the pristine nanowires and to verify that silicon nanowires had grown on the sample.

### 11.2 Experimental Details

Both uncoated glass and ITO-coated aluminosilicate glass were used for different parts of this work. Where a transparent and conductive layer was needed, the ITO was used. For other samples, the presence of a conductive layer was undesirable and for these, uncoated glass was used. These substrates were cleaned by the method outlined in Chapter 4 before being transferred into a vacuum system for deposition of the catalyst layer.

Gold and tin catalysts were used for the growth of silicon nanowires via the VLS mechanism. Catalyst films were kept at a constant 100nm in thickness for most samples with a thicker catalyst layer being used in several other trials. As shown in previous chapters, gold and tin are catalysts that produce a high coverage of nanowires. Tin was used as it tends to produce nanowires of a different morphology, thinner nanowires and at a higher density to those grown using a gold catalyst.

Silicon nanowires were grown at high density using Pulsed PECVD (PPECVD) at a temperature of approximately 345°C. Silane was used as a source of silicon for VLS growth of the silicon nanowires. A square wave produced by a pulse generator (SRS Model DG535) was used to modulate the 13.56MHz signal used to generate the plasma. A modulation frequency of 1000Hz was used and the mark space ratio was held at a constant ratio of 1:1. The sample was allowed to heat up under 3.0 torr of Argon for 35 minutes and for a further 35 minutes under the mixture of reactant gasses. The silicon nanowires were produced using silane slightly diluted in argon (70% silane) and a plasma duration of 40 seconds. Doped nanowires (p-type) were produced by using diborane (1% in argon) in place of the argon. After the period of PPECVD, the plasma was switched off but gas flow and temperature
were maintained allowing a further period of CVD of 10 minutes to aid the nanowire growth. As shown in Chapter 9 this period of CVD does increase the coverage of the silicon nanowires, although not as large an extent as the initial few seconds of PPECVD.

Several different layers were used in creating the devices in this work. All of the layers were deposited within the one chamber. The amorphous silicon layers (p, n and intrinsic) were deposited at a temperature of 225°C and a chamber pressure of 0.7 torr. PECVD was used to deposit the amorphous silicon layers at a typical plasma power of 4W. Undiluted silane was used to create the intrinsic amorphous silicon layer and a deposition time of 25 minutes was used for all the intrinsic amorphous silicon layers. To create the p-type amorphous silicon layer, the silane (100%) was mixed with diborane (1% in argon) and a deposition time of 23 seconds was used. The n-layer was produced over 3 minutes using a gas mixture of phosphine (1% in argon) and silane (100%). The doping ratios of the p-layer and n-layer as well as the thickness of the layers were kept consistent with the ratios used for thin film amorphous silicon photovoltaic devices.

A variety of different devices were created using the doped and intrinsic amorphous silicon layers and the intrinsic silicon nanowires. The variants are listed in Table 11-1. Also listed in Table 11-1 are the efficiency, fill factor, short circuit current and open circuit voltage for each device.
To describe the device structures in this chapter the following abbreviation conventions will be used:

- NW refers to a thin film of nanowires.
- [Au/Sn] refers to a catalyst layer.
- Where a specific catalyst is used it is referred to as either Sn or Au.
- [NW] is a layer of amorphous silicon that was deposited at the same temperature and conditions at which nanowire growth occurs.
- The amorphous silicon layers are labelled as p, i and n.
- The p-type nanowires are referred to as pNW.
- The ITO and aluminium layers are referred to as ITO and Al respectively.

To further aid the description of the device structures schematics of the devices are shown inset within each IV characteristic. These show the plan view and a cross-section showing the layer structure of each of the devices. Measurements of the layer thicknesses are included where known.

Intrinsic silicon nanowires were produced on both ITO and uncoated glass. In the case of the ITO samples a back-contact was deposited on top of the nanowires. The size of each contact and hence the device itself was 0.045cm\(^2\). A control sample was present in these tests which underwent the same treatment but did not have the gold catalyst. Therefore no nanowire growth occurred on these samples.
Table 11-1: Devices and properties thereof produced using doped a-Si:H and intrinsic silicon nanowires. Devices marked with * did not have any nanowires or nanowire growth did not occur.

<table>
<thead>
<tr>
<th>Nanowire Catalyst</th>
<th>Order of layers</th>
<th>Efficiency (%)</th>
<th>Fill Factor (%)</th>
<th>( V_{oc} ) (mV)</th>
<th>( I_{sc} ) (µA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Au NW</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>Au NW-n</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Au NW-p-i-n</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Au p-NW</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Au p-NW-i</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Au p-NW-i-n</td>
<td>negligible</td>
<td>negligible</td>
<td>70</td>
<td>~1</td>
<td></td>
</tr>
<tr>
<td>Au p-NW-n</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Au p-i-n-NW *</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>N/A p-i-n *</td>
<td>3</td>
<td>44</td>
<td>780</td>
<td>380</td>
<td></td>
</tr>
<tr>
<td>Sn NW</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Sn NWn</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Au p-NW-n (transverse)</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Au pNW-i-n</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Sn pNW-i-n</td>
<td>0.031</td>
<td>55</td>
<td>390</td>
<td>3.8</td>
<td></td>
</tr>
</tbody>
</table>

After the deposition the system was purged with argon and cooled to near room temperature, the samples were then removed for further treatment. Back-contacts, or a series of Al contacts, were placed on the sample using the thermal evaporation system so that the electrical characteristics could be measured.

Once the contacts were in place the IV characteristics of the samples under dark and illuminated conditions were measured. Some of the samples were then mounted on SEM stubs for measurement using a ZEISS 1555 VP FESEM to verify the presence of silicon nanowires.
11.3 Results
A variety of silicon nanowire thin film samples were created and analysed. The results are presented using IV characteristics of the samples. Some samples were examined using FESEM to verify there were silicon nanowires present. The results are broken up into sections dealing with each variant of silicon nanowire thin film device that was produced.

11.3.1 Transmittance Measurements
Transmittance measurements were taken for silicon nanowire thin films grown using gold or tin as a catalyst. They clearly show that the material effectively absorbs visible and UV light, as shown by the transmittance measurements in Figure 11-1 and Figure 11-2. However, it must be noted that these films are much thicker in regions where the nanowires are overlapping each other than the more transparent amorphous silicon thin films (~540nm) used for amorphous silicon photovoltaic devices. The average thickness of the gold-catalysed nanowire layer is estimated to be ~70µm and the thickness of the tin-catalysed nanowire film is estimated to be ~20µm. The transmittance measurements for a typical amorphous silicon device are shown in Figure 11-3. This extremely low transmittance across the visible spectrum, UV (~375nm to ~8.8nm (Hecht, 2002)) and particularly into the near IR (780nm to 3000nm (Hecht, 2002)), for the silicon nanowire samples in comparison to the amorphous silicon film is of interest in relation to the absorption of light within the device.
Figure 11-1: Ultraviolet and visible spectroscopy transmittance measurements for a gold-catalysed silicon nanowire film.

Figure 11-2: Ultraviolet and visible spectroscopy transmittance measurements for a tin-catalysed silicon nanowire film.
11.3.2 Nanowire Based Devices
The following series of samples use a thin film of undoped silicon nanowires as a main component. The dopant layers, where they were used, were made of doped amorphous silicon. The combination of layers ranged from just intrinsic silicon nanowires to p-i-n junctions which used silicon nanowires as the i-layer. The samples were investigated for photoconductivity and photocurrent.

11.3.2.1 ITO-[Au/Sn]-NW-Al
The IV characteristics of the intrinsic silicon nanowire samples exhibited a non-linear form. In Figure 11-4 it can be seen that the resistance of the nanowires was much higher than that of the parasitic amorphous silicon growth in Figure 11-5. That is, silicon nanowire thin films are much more resistive than the amorphous silicon deposited during the growth of the
nanowires. The difference in this resistance varied by up to a factor of 10 between samples but was consistently greater than the amorphous silicon control sample. From Figure 11-4 it can also be seen that the nanowires are photoconductive. That is, the conductivity increased under illumination. This can be seen by the increase in current for a bias-voltage when the sample was illuminated. The amorphous silicon samples that were grown in the same conditions as the nanowires exhibited no photoconductivity over the data range examined.

Figure 11-4: IV curve for silicon nanowires between ITO and an Al contact (ITO-Au-NW-Al). Illumination provided by an approximately AM1 halogen lamp light source. The inset schematic shows the device layout and layer structure.
The resistance of amorphous silicon sample produced under the same conditions, but without a catalyst, had a lower resistance than the nanowire sample. The IV characteristics of the high temperature amorphous silicon are shown below in Figure 11-5.

Figure 11-5: IV curve for an intrinsic amorphous silicon deposited during nanowire growth phase between ITO and an aluminium contact (ITO-[NW]-Al). The inset schematic shows the device layout and layer structure.
Nanowires catalysed with a tin catalyst were slightly different. As can be seen in Figure 11-6 below, the Sn-catalysed nanowire samples are much more conductive and have a much greater curvature, indicating a non-ohmic characteristic, than the gold-catalysed nanowires. This sample is also photoconductive, that is, under illumination the conductivity of the sample increases.

Figure 11-6: Nanowires produced with a tin catalyst between ITO and an aluminium contact (ITO–Sn–NW–Al). The inset schematic shows the device layout and layer structure.
11.3.2.2 Al-[Au/Sn]-NW-Al

The IV characteristics were measured for the situation where the nanowires were deposited on glass with two contacts deposited on top of the nanowires at 6.75mm from each other. A schematic of this sample is shown in Figure 11-7.

![Schematic of a silicon nanowire thin film on glass with aluminium contacts.](image)

The nanowire sample had a much more linear IV characteristic with a measurable resistance of 70 kΩ to as high as 1.5 MΩ depending on the sample. The IV characteristic of this sample is shown in Figure 11-8.
11.3.2.3 ITO-[Au/Sn]-NW-n-Al

Devices were created where an intrinsic nanowire layer was coated with a doped amorphous silicon layer (n-type) producing an NW-n device. A sample produced without the catalyst was also present during the deposition so the characteristics of the amorphous-only device could be observed. The resistance of the nanowire device as seen in Figure 11-9 was much higher than the equivalent without nanowires as can be seen in Figure 11-10. The data for this graph has been slightly smoothed, as described in Chapter 4. However, due to the low signal strength some noise is still apparent in the chart. As can also be seen both devices, with and without the nanowires, show a conductivity increase when exposed to light. Both materials also exhibit non-ohmic behaviour as illustrated by the slight upward curve in the IV characteristics.
characteristics. The curves within each line are an artefact of the high signal noise and smoothing process.

Figure 11-9: IV curve for gold-catalysed silicon nanowires and n-layer amorphous silicon between ITO and an aluminium contact (ITO-Au-NW-n-Al) (smoothed data). The inset schematic shows the device layout and layer structure.
Chapter 11: Silicon Nanowire Devices

Figure 11-10: IV curve for amorphous silicon deposited during nanowire growth phase (no catalyst) and n-type amorphous layer (ITO-[NW]-n-Al). The inset schematic shows the device layout and layer structure.

Similar to the characteristics of the pristine nanowires, the tin-catalysed silicon nanowires also showed a lower resistance than the gold-catalysed nanowires. The characteristics in Figure 11-11 showed an increase in conductivity when the sample was illuminated compared to the dark characteristic. The IV characteristic of the sample with tin-catalysed nanowires more closely resembles the characteristic of the sample without nanowires, as it had a stronger non-ohmic behaviour than the Au-NW-n sample.
Figure 11-11: IV characteristics for tin-catalysed nanowires coated with an amorphous silicon n-layer (ITO-Sn-NW-n-Al). The inset schematic shows the device layout and layer structure.

11.3.2.4 ITO-[Au/Sn]-NW-p-i-n-Al

A set of samples was produced where a nanowire layer was deposited on ITO followed by an amorphous silicon p-i-n junction, from a recipe used to create solar cells of $\eta \sim 2\%$ (Parlevliet, 2004). By placing nanowires before the p-i-n junction it was hoped to improve light trapping. The IV characteristic of the sample with nanowires showed that they were highly resistive. The measurements resembled an open circuit IV curve. That is, the sample was not conductive over the voltage range measured. Thus, no photoconductive or photovoltaic effects were observed.
An SEM micrograph is shown in Figure 11-12a. This exhibits unusual charging effects due to the presence of the p-i-n coating. The amorphous material on the sample with no catalyst, Figure 11-12b, showed an unexpectedly textured surface. This resembled an opal like structure in comparison to the largely featureless amorphous silicon surface usually observed. This structure was likely due to the high temperatures used during its growth as it was exposed to the same conditions that grew the silicon nanowires. This was an unexpected structure as amorphous silicon samples are usually fairly flat and featureless.

Figure 11-12: SEM micrographs of a) Silicon nanowires coated with a p-i-n junction (ITO-Au-NW-p-i-n-Al) and b) the sample present during deposition without a catalyst (ITO-[NW]-p-i-n-Al).
The IV characteristic of the opal like structure shown in Figure 11-12b is shown below in Figure 11-13. These samples exhibited a photovoltaic effect although the efficiency was extremely low at 0.03%. This was due to the combination of a low open circuit voltage (0.495V) as compared to the more normal amorphous silicon value of 0.8V, a low fill factor of 22.2% and very small photocurrent. The shunt resistance was very small at 12.8kΩ.

![Figure 11-13: IV characteristic for the opal like structure with an amorphous p-i-n junction of Figure 11-12b (ITO-[NW]-p-i-n-Al). The inset schematic shows the device layout and layer structure.](image-url)
11.3.2.5 ITO-[Au/Sn]-p-NW-Al

It was found that nanowires could be grown through a thin amorphous p-layer. That is, a gold catalyst layer was deposited followed by an amorphous p-layer. The sample temperature was then raised to the point where nanowire growth could occur. As seen by the higher current flow in the sample shown in Figure 11-14, the nanowire films grown via this process have a resistance several orders lower than that of the intrinsic nanowires or those with an n-layer on top of the nanowires. However, no photo-response was observed and the characteristic was ohmic. This lack of photoconductivity would be expected as the device is behaving as a short. Any change in photoconductivity is not likely to have a big influence on the characteristics. The resistance of these nanowires was 155Ω.

![Figure 11-14: IV characteristics of silicon nanowires grown through an amorphous p-layer (ITO-Au-p-NW-Al). The inset schematic shows the device layout and layer structure.](image-url)
The characteristics of the sample exposed to the same conditions without the catalyst are markedly different. As seen in Figure 11-15, the characteristics are non-ohmic and have a much higher resistance than the sample containing the nanowires. This sample exhibited photoconductivity but not photovoltage or photocurrent.

*Figure 11-15: IV characteristics of an amorphous p-i device (ITO-p-[NW]-Al). The inset schematic shows the device layout and layer structure.*
11.3.2.6 ITO-[Au/Sn]-p-NW-i-Al

A series of samples was produced to observe what effect having an intrinsic amorphous layer deposited on top of the nanowire layer would have. The net result, as shown in Figure 11-16 below, was to increase the resistance of the sample and enhance the photoconductive effect. It is also of note that the characteristics are not as clearly ohmic as those of the nanowire sample in Figure 11-14. Instead they showed a slight curvature. There is also a hint of photovoltage from the sample and a strong photoconductive effect.

Figure 11-16: IV characteristic for a p-NW-i device (ITO-Au-p-NW-i-Al). The inset schematic shows the device layout and layer structure.
The sample exposed to the same growth conditions but without a gold catalyst showed similar characteristics to that of the sample shown in Figure 11-15 but without as much curvature, as seen in Figure 11-17. However, a strong photoconductive effect is evident. This is probably a result of the thick amorphous silicon i-layer.

![Figure 11-17: IV characteristic for an amorphous p-i device (ITO-p-[NW]-i-Al). The inset schematic shows the device layout and layer structure.](image)

### 11.3.2.7 ITO-[Au/Sn]-p-NW-i-n-Al

To develop a photovoltaic device with an increased potential difference across the junction, an amorphous n-layer was deposited on top of the p-NW-i device to produce a p-i-n device with nanowires embedded within the i-layer. Some samples measured showed ohmic characteristics while a number showed diode characteristics. One such characteristic is shown below in Figure 11-18. This device shows an IV characteristic similar to what is expected for a solar cell with the exception that there was no significant photocurrent observed. However,
it can be seen that there is only a slight displacement of the illuminated curve from the dark curve at the origin. This led to an open circuit voltage of approximately 70mV, a short circuit current of $\sim 1\mu A$ and a negligibly small efficiency. It must be noted that this effect could be due to the regions between the nanowires, or in low density areas, where an amorphous p-i-n layer may have been formed without nanowires present.

A sample that was exposed to the same conditions but without the presence of a catalyst layer showed an unusually poor conductivity. This sample also appeared similar in texture and morphology to that shown in Figure 11-12b. The characteristic of this sample is shown in Figure 11-19. The data for this graph has been slightly smoothed, as described in Chapter 4. However, due to the low signal strength some noise is still apparent in the chart. The

Figure 11-18: IV characteristic of a p-NW-i-n device (ITO-Au-p-NW-i-n-Al). The inset schematic shows the device layout and layer structure.
sample shows a photoconductive response, the shape expected for a photovoltaic device, a low shunt resistance and negligible photocurrent. Although there is a slight displacement of the illuminated curve as there was in the sample shown in Figure 11-18, the \( I_{SC} \) and \( V_{OC} \) were extremely low. This was likely due to the high temperatures to which the amorphous silicon p-layer was exposed during the nanowire growth phase compromising the quality of the p-layer. Alternatively, the doped amorphous silicon comprising the p-layer could have been absorbed into the nanowire during its initial growth. This is because the silicon would have been absorbed by the gold droplet during the formation of the eutectic. The thickness and high resistivity of the nanowire intrinsic layer would also be detrimental to the amount of photocurrent generated by this device.

![IV characteristic for an amorphous p-i-n device](image)

*Figure 11-19: IV characteristic for an amorphous p-i-n device with a part of the i-layer deposited at the high temperatures present during nanowire growth (ITO-p-[NW]-i-n-Al) (smoothed data). The inset schematic shows the device layout and layer structure.*
11.3.2.8 ITO-[Au/Sn]-p-NW-n-Al

A device was produced that was similar to the p-NW-i-n device but without the additional amorphous i-layer. The results showed an ohmic characteristic and no photocurrent. This can be seen in Figure 11-20. The resistance of this device was 212Ω over the voltage range measured. No change in the conductivity was observed under illumination. This lack of photocurrent and photoconductivity would likely be due to the poor quality of the p-layer due to the high temperatures used and the absorbance of this material into the nanowires during their growth. However, as this device is behaving as a short any change in photoconductivity is not likely to have a big influence on the characteristics so there would be no measurable photoresponse. The i-layer itself would be of poor quality as the nanowire layer is highly resistive.

Figure 11-20: IV characteristic for a p-NW-n device (ITO-Au-p-NW-n-Al). The inset schematic shows the device layout and layer structure.
A device was produced without a catalyst and was exposed to the same conditions as in Figure 11-20. It proved to be photoconductive, as seen in Figure 11-21, and it also exhibited a strong diode characteristic. However, it was not a photovoltaic device. This device, without the highly resistive nanowire layer, showed photoconductance. The lack of any photocurrent would be due in part to the high temperatures to which the p-layer was exposed during the growth phase.

![Graph](image)

**Figure 11-21:** IV characteristic for an amorphous p-i-n device with the i-layer deposited at high temperatures during nanowire growth (ITO-p-[NW]-n-Al). The inset schematic shows the device layout and layer structure.

To summarise these results, intrinsic silicon nanowires using gold as a catalyst exhibited photoconductivity and a diode-like characteristic. Using tin as a catalyst resulted in similar characteristics. However, the tin-catalysed nanowires tended to be more conductive and the
diode characteristic was stronger. The addition of an n-type amorphous silicon layer to the tin-catalysed silicon nanowires produced samples with diode-like characteristics and that were photoconductive. However, the samples for both gold and tin-catalysed nanowires were less conductive than the samples without the n-layer. Growing the nanowires on top of an amorphous silicon p-layer produced samples that were ohmic and they did not exhibit photoconductivity. Samples produced with both the amorphous p-layer and n-layer were also ohmic and were not photoconductive. These samples, although not photovoltaic, show that the silicon nanowires are an intrinsically photoconductive structure that can exhibit diode characteristics. The addition of an amorphous intrinsic layer to produce p-NW-i structures created devices that were photoconductive, had good diode characteristics and produced a small photovoltage. Adding an amorphous n-layer to the p-NW-i structure resulted in devices which were photoconductive and photovoltaic but with a stronger diode characteristic. These last two device designs showed the greatest potential as solar cells when silicon nanowires were used as an i-layer.

11.3.3 Modified Amorphous Silicon Devices
To observe the affect that depositing a nanowire layer on the back of a p-i-n device would have several samples were produced. The rationale behind these samples was to improve the scattering of light within the device in order to improve absorption. The amorphous silicon p-i-n device was deposited first. For each batch of samples, one sample had back-contacts added and was analysed, one was coated with a gold layer and the third was left as it was. The coated and uncoated samples were then placed back in the chamber for the NW growth phase. It was found that there was no nanowire growth on the samples with the catalyst. This has been observed previously. Nanowires do not grow on top of thick amorphous silicon layers. The p-i-n device was relatively thick at ~500nm. All three samples had morphologies similar to the plain amorphous film of the p-i-n device.
A micrograph of the amorphous p-i-n device is shown in Figure 11-22, which had been coated in an aluminium film. It should be noted that although there is some surface texturing, it is not textured to the same extent as the material shown in Figure 11-12b.

Figure 11-22: SEM Micrograph of an amorphous silicon p-i-n device (ITO-p-i-n-Al).
The IV characteristic of an amorphous p-i-n device is shown below in Figure 11-23. This device had an efficiency of 3% with a fill factor of 44%. Under optimised growth conditions simple single junction amorphous devices have been grown with an efficiency of up to 3.8% in the PECVD system at Murdoch University (Parlevliet, 2004).

![IV characteristic of an amorphous p-i-n junction after deposition at 225°C (ITO-p-i-n-Al). The inset schematic shows the device layout and layer structure.](image)

The sample without a catalyst had the same surface morphology as the amorphous p-i-n device. This sample was left in the chamber while the nanowires were grown. The IV characteristic for this sample shows a low conductivity for both the dark and illuminated measurements as compared to the amorphous p-i-n without the high temperature treatment shown in Figure 11-23. The sample without a catalyst, although photoconductive, was no longer a photovoltaic device. This can be seen in Figure 11-24. The high temperature to
which this device was exposed during the nanowire growth phase (~340°C), the equivalent of a high temperature anneal, has compromised the quality of the device. In addition, a poor quality amorphous i-layer deposited during nanowire growth with many defects leads to a lowered shunt resistance.

Figure 11-24: IV characteristics for an amorphous p-i-n device exposed to nanowire growth conditions (ITO-p-i-n-[NW]-Al). The inset schematic shows the device layout and layer structure.
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The samples which were coated with a gold catalyst did not yield any nanowire growth. The IV characteristics of these samples were measured despite this. The characteristics shown below in Figure 11-25 show a very low conductivity of the sample. There was a slight conductivity change between the dark and illuminated samples. However, any photovoltaic effect was small and masked by the instrumentation noise.

![Figure 11-25: IV characteristics for an amorphous p-i-n device coated with Au and exposed to nanowire growth conditions (ITO-p-i-n-Au-[NW]-Al). The inset schematic shows the device layout and layer structure.](image)

11.3.4 Transverse Al-p-[Au/Sn]-NW-n-Al
To avoid exposing the doped amorphous p-layer to the high temperatures required for nanowire growth, a transverse device was produced. This design involved a glass substrate upon which a strip of gold 5mm wide was placed using a shadow mask. The sample was then placed in the PECVD system and the nanowires were allowed to grow. The sample was then
removed from the chamber and masked so that only a region 3mm wide and an overlapping 1mm of the nanowire strip was left clear. The sample was then placed back in the PECVD system and an amorphous p-layer deposited. The sample was then removed and the mask relocated so that the other side of the nanowire strip was exposed. An amorphous n-layer was then deposited on this region. Finally, the sample was moved to a separate system where aluminium contact strips were placed overlapping 2mm of the doped amorphous strips. This structure and the steps taken for growth are shown in Figure 11-26.

![Figure 11-26: Schematic of the transverse nanowire device and the steps used in its growth.](image)
The IV characteristics of the samples, one of which is shown in Figure 11-27, show that the device is highly resistive. This is likely due to the distance across the junction. However, a slight diode characteristic was apparent but it was unclear whether a photoconductive effect or photovoltaic effect was present due to the low signal level and low signal to noise ratio.

![Figure 11-27: IV characteristic for a transverse p-NW-n device (Al-p-Au-NW-n-Al). The inset schematic shows a cross-section of the layer structure.](image)

**11.3.5 Nanowires as a Dopant Layer ITO-[Au/Sn]-pNW-i-n-Al**

It was found in Chapter 9 that nanowires would not grow with a useable density when the silane partial pressure was below ~1.5 torr. For the same dopant ratios used for creating amorphous silicon devices, the partial pressure of silane in a chamber at a total pressure of 3.0 torr would need to be less than 0.6 torr. Producing a doped nanowire p-layer using the low dopant ratio that ensures good nanowire growth would result in a very lightly doped p-layer compared to these amorphous silicon standards. However, although only a lightly
doped layer could be produced, using these p-type nanowires as part of a p-i-n photovoltaic device was investigated. A substrate-p-i-n device was produced as it was the standard structure used to produce the amorphous silicon photovoltaic devices at Murdoch University. However, it would also be possible to grow n-type silicon nanowires using a similar method. This would allow substrate-n-i-p devices to be produced, using nanowires as an n-layer.

Devices were produced using gold-catalysed p-type nanowires which were coated in an intrinsic amorphous silicon layer and an n-type amorphous silicon layer. Under the growth conditions used, nanowires nucleated and grew before being coated in amorphous silicon layers. The subsequent nanowires are very thick in appearance as shown in Figure 11-28.

Figure 11-28: SEM micrograph of gold-catalysed p-type silicon nanowires coated in amorphous silicon intrinsic and n-layers (ITO-[Au]-pNW-i-n-Al).

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This device, although being photoconductive and having a diode characteristic, did not generate any photocurrent. The IV characteristic for this device is shown in Figure 11-29. In regions of the sample, where nanowire growth was patchy with the dominant growth being the opal-like structures shown in Figure 11-12b, the sample did show a photocurrent. This would be due to the purely amorphous silicon p-i-n layers deposited in these regions. The addition of the highly textured nanowire p-layer was actually detrimental to the collection efficiency of the device.

Figure 11-29: IV characteristics of a device using gold-catalysed p-type nanowires with an amorphous intrinsic and n-layer (ITO-[Au]-pNW-i-n-Al). The inset schematic shows the device layout and layer structure.
Devices of the same structure, pNW-i-n, were produced using a tin catalyst to keep the film thickness to a minimum. The nanowires produced had the ‘knotted’ morphology described for tin-catalysed nanowires in Chapter 7. When coated in the amorphous silicon layers, these nanowires became very ‘worm-like’ in appearance as shown in Figure 11-30.

![SEM micrograph of tin-catalysed p-type silicon nanowires coated in amorphous silicon intrinsic and n-layers (ITO-[Sn]-pNW-i-n-Al).](image)
Chapter 11: Silicon Nanowire Devices

This device was both photoconductive and photovoltaic. It displayed a measurable photocurrent when illuminated. An IV characteristic of this device is shown in Figure 11-31. The efficiency of this device was found to be 0.031% with a $V_{OC}$ of 0.39V, $I_{SC}$ of 3.8µA and a high shunt resistance.

![Figure 11-31: IV characteristics of a device using tin-catalysed p-type nanowires with an amorphous intrinsic and n-layer (ITO-[Sn]-pNW-i-n-Al). The inset schematic shows the device layout and layer structure.](image)

Figure 11-32 shows a comparison between the IV characteristics of the silicon nanowire device shown in Figure 11-31, an amorphous silicon solar cell (Parlevliet, 2004), a crystalline silicon standard cell and the single silicon nanowire device produced by Tian and co-workers (2007). The axes of this graph have been normalised to a ratio of the maximum voltage and current. The crystalline silicon solar cell, amorphous solar cell and the nanowire thin film solar cell grown in this work were all measured on the same IV characterisation system. From
Figure 11-32 the differences in fill factor can be readily observed. The crystalline silicon solar cells had the highest fill factor. The two nanowire devices and the amorphous silicon solar cell all had fill factors of ~55%. The nanowire devices are fairly similar in characteristics, although the nanowire thin film solar cell grown in this work had a slightly larger series resistance. In comparison to the amorphous silicon solar cell, the nanowires had a smaller shunt resistance.

Figure 11-32: Normalised IV characteristics of amorphous silicon, crystalline silicon and silicon nanowire solar cells.
11.3.6 Coaxial Nanowire Morphology

The morphologies of the nanowires that had been coated with layers of amorphous silicon and aluminium were examined using an SEM to determine if the nanowires were of a coaxial form similar to that described by Tian, Zheng and coworkers (2007). By coating the nanowires in polycrystalline silicon they observed a core like morphology at the end of the nanowires (Tian et al., 2007). To determine if the nanowires produced in this project had a similar morphology, nanowires from a p-NW-i-n device were scraped from a region coated in aluminium onto an SEM stub covered with carbon tape. This was done to fracture the nanowire in order to observe if a coaxial morphology was evident at the ends of the nanowires. Figure 11-33 shows the ends of several nanowires that exhibit a coaxial like morphology. Figure 11-33a shows the catalyst tip end of a nanowire. In this image no rings can be seen. In Figure 11-33b, c and d, the different compositional rings of the nanowires can be seen. In this situation the inner core would consist of an intrinsic silicon nanowire surrounded by a relatively thick intrinsic amorphous silicon layer. A thin n-type amorphous silicon layer would then be present surrounded by a thick Al layer. This morphology is similar to that shown by Tian and co-workers (2007).
**Figure 11-33: Coaxial morphologies in silicon nanowires** a) a catalyst tip with no ring structure. b), c) and d) show layers of different material surrounding the nanowire. Scale bars are all 200nm.

### 11.4 Discussion

Silicon nanowires have been used, along with amorphous silicon, as a test bed for silicon nanowire based photovoltaics. The transmittance measurements shown in Figure 11-1 and Figure 11-2 indicate that thick films of nanowires absorb large portions of the visible spectrum and into the near IR. It must be noted when compared to the amorphous silicon shown in Figure 11-3 that the nanowire film would be thicker on average and have large variations in thickness across the substrate. Although the nanowires are essentially randomly aligned, there would be regions of the film where many nanowires are overlapping each other or growing nearly vertically, creating a thick film. Other regions between the nanowires,
would exist where the film thickness is solely due to the parasitic amorphous silicon growth during deposition. With the nanowire densities used, these patches between nanowires would be separated by several hundreds of nanometres of the same scale as the wavelengths of visible light. This would aid light trapping within the material. As such, the transmittance measurements indicate that the nanowire films trap a large portion of the light incident upon them.

Silicon nanowire thin films were found to be much more resistive than the un-catalysed amorphous silicon deposited during the growth conditions used to produce silicon nanowires. Tin-catalysed silicon nanowires were found to be more conductive than the gold-catalysed silicon nanowires produced under the same growth conditions. This is likely due to the thicknesses of the films in question. Each of the nanowire layers was substantially thicker than the un-catalysed amorphous silicon layer. The gold-catalysed silicon nanowires had an approximate film thickness of 70µm while the tin-catalysed silicon nanowires had a film thickness of approximately 20µm. This difference in film thickness would help to account for the difference in resistance of the samples.

Undoped silicon nanowires have previously been shown to be slightly p-type (Chung et al., 2000). This would aid in the conductivity measurements as a readily measurable current would flow due to the presence of charge carriers in the material. The nanowires in Figure 11-4 for Au-NW and Figure 11-6 for Sn-NW show non-ohmic characteristics. This is likely due to the presence of a Schottky diode at the interface between the nanowires and the ITO. The Schottky diode at this interface was expected due to the presence of free indium. The indium was produced during the disproportionation of the ITO at the nanowire growth temperature. It is worth noting that the purely amorphous silicon sample did not show this characteristic.
The nanowire sample on a glass substrate showed no diode characteristics and exhibited a linear increase in current flow as the voltage was raised. When an amorphous n-layer was added to the silicon nanowires the resulting IV characteristics showed diode behaviour. For the sample without nanowires this diode behaviour was a pronounced characteristic, while for the nanowire sample it was of reduced strength. This was likely due to the high resistance of the nanowire material suppressing the current signal. The diode characteristic in these samples is likely to be influenced by the same Schottky effects that were present in the nanowire samples in Figure 11-4 and Figure 11-6. However, the slightly p-type nature of the nanowires and the n-type amorphous material would form a weak p-n junction, contributing to or decreasing the diode characteristic.

By adding a p-layer before the nanowires, the IV characteristics of the samples showed a much more linear response, as seen in Figure 11-14, and had no photoresponse. However, the IV characteristics of the amorphous-only sample showed strong diode characteristics. Adding an i-layer to the nanowires produced an increased photoresponse in the nanowire sample without significantly increasing the diode characteristic. The lack of photoresponse, or measurable change in photoconductivity of some devices was understandable as the devices were behaving as electrical shorts. That is, the current flowing through the device was high enough that any change in conductivity under illumination would not be measurable.

The diode characteristics of the silicon nanowire samples were improved by the addition of an n-type amorphous silicon layer to the nanowires embedded in an amorphous i-layer with a p-type amorphous under-layer. The diode characteristic was much stronger as shown in Figure 11-18. The samples of this structural type were the only nanowire based samples to show a significant photovoltaic behaviour. The sample had an open circuit voltage of approximately 70mV, a short circuit current of ~1µA and a negligibly small efficiency. This effect could be due to the regions between the nanowires or in low density areas where an
amorphous p-i-n layer may have been formed without nanowires present. However, the amorphous-only device deposited in tandem with the nanowire device did not show a significant photovoltaic effect. This indicates that the nanowire sample was indeed generating a photocurrent. This low efficiency was likely because of the degradation of the amorphous p-layer due to the high temperatures involved in nanowire growth and the associated migration of dopants. When a sample was produced without the intrinsic amorphous layer, the IV characteristics of the nanowire sample once again became linear as shown in Figure 11-20. This would indicate that much of the conduction of the minority carriers within the device was within the amorphous matrix rather than the nanowires themselves. The removal of this layer thus results in an apparent overall increase in the resistivity of the device, obscuring the diode characteristic. The amorphous-only sample still showed a strong diode characteristic.

An attempt was made to grow silicon nanowires on the back of an amorphous p-i-n device. This was unsuccessful as the silicon nanowires would not grow on thick amorphous silicon layers. The basic amorphous p-i-n device can be seen in Figure 11-23. This device only had a 2% efficiency, due in part to oxidation of the n-layer caused by the removal of the sample to atmosphere at a reasonably high temperature. This oxidation resulted in a distinct kink in the IV characteristic at \( V_{OC} \). The samples that were placed back in the chamber and exposed to nanowire growth conditions both showed diode characteristics with a much higher overall resistivity. Interestingly, the sample with a gold layer on it had a higher resistivity than the sample without. Neither sample showed a photovoltaic effect. This was likely due to the high temperatures involved in the nanowire growth causing the dopants to migrate within the device. The addition of a layer of high temperature amorphous silicon to the back of the p-i-n junction was also likely to reduce the efficiency and diode characteristics of the device. As the high temperatures involved in the deposition of the silicon nanowires was likely to damage the doped amorphous silicon layers, a transverse design was trialled.
A transverse device was created where the silicon nanowires were grown before the amorphous p-layer and n-layer were deposited using shadow masks. This involved breaking the vacuum between steps allowing oxidation of the nanowires before the doped layers were put down. Although highly resistive, the transverse device did show a slight diode characteristic due to the dopant layers or a Schottky diode at the contacts. However, the resistivity of the device was extremely high, rendering it difficult to observe any photovoltaic or photoconductive effect. This high resistivity of the device was due to the extreme size of the device. With an intrinsic nanowire layer ~3mm across between the doped regions, the minority carrier lifetime would not be long enough to generate a significant photocurrent. If more appropriate masking or lithographic techniques were used to reduce the active region of this device to < 500nm, on par with the thickness of an amorphous silicon thin film device, an observable photocurrent would be expected.

A functioning solar cell was produced by lightly doping tin-catalysed nanowires and using them as a p-layer in an amorphous silicon device. This had a very low efficiency when compared with the standard amorphous silicon devices. This low efficiency is partly due to the lightly doped p-layer. A low ratio of dopant gas to silane was used in order to produce a high density growth of silicon nanowires. For higher dopant gas to silane ratios, or lower silane partial pressures, the density of the nanowires decreased as discussed in Chapter 9. For more strongly doped nanowires the device should become more efficient. A different method of doping would need to be investigated or modifications made to the deposition system as increasing the dopant ratio even slightly resulted in samples with very few nanowires. A second reason for this low efficiency is the thickness of the p-type nanowire layer. This layer is very thick in comparison to the p-type amorphous silicon layer normally used which would result in poor electron transport out of the device. Where an even thicker nanowire layer, using gold-catalysed nanowires, was used, the device no longer produced a measurable photocurrent. As both the tin-catalysed and gold-catalysed samples were
deposited under identical conditions the only difference is the morphology of the nanowire layer. As was mentioned in Chapter 7 and shown in Figure 7-11 the gold-catalysed nanowires produced a much thicker film than the tin-catalysed nanowires. This helps to explain the difference in photocurrent between the two samples. The low current could also be due to only a limited number of the nanowires contributing to the photocurrent. Only limited numbers of nanowires would have been in direct contact with the measurement probe and defects within the wires may be contributing to current losses. The $V_{oc}$ was also significantly lower ($\sim0.4V$) than that for an amorphous silicon device ($\sim0.8V$). This could be due to both the dopant profile and crystalline content of the nanowires as crystalline silicon solar cells tend to have a lower $V_{oc}$ than their amorphous silicon counterparts. The fill factor of the device, when averaged over a large number of measurements, was found to be very similar to the average fill factor of the amorphous silicon solar cells that were produced on the same system. The fill factor was also very similar to that of the single nanowire device produced by Tian and co-workers (2007). The $V_{oc}$ of the thin film silicon nanowire device was larger than that of Tian and co-workers (2007). The use of amorphous silicon rather than microcrystalline may be in part contributing to the higher $V_{oc}$. This prototype device demonstrates that silicon nanowires can be used in photovoltaic devices, albeit some optimisation is necessary to improve the device.

The silicon nanowires grown in this work were found to have an observably coaxial morphology. That is, a central silicon nanowire core surrounded by amorphous silicon and aluminium layers. The core structure can be seen on the nanowires in Figure 11-33b, c and d. Figure 11-33a illustrates the end of a nanowire with a catalyst tip coated in the various layers for comparison. It shows that the observed core structure was the internal structure of the nanowire, as seen from the broken end. This structure was very similar to that described by Tian, Zheng and coworkers (2007). The structure of the nanowires in this project consist of an intrinsic nanowire core wrapped in an i-type amorphous silicon sheath with a further n-
type amorphous silicon coating and a final aluminium coating. A similar photovoltaic effect to that observed by Tian, Zheng and coworkers (2007) could be measured with appropriate techniques. The essentially intrinsic silicon nanowires are known to be naturally slightly p-type (Chung et al., 2000). This would result in a weak photovoltaic effect. If p-type silicon nanowires were used as a central core, similar results to Tian, Zheng and co-workers would be expected. This was shown with the samples produced using a lightly doped silicon nanowire p-layer with amorphous silicon i-layers and n-layers. Amorphous silicon sheaths would have an advantage over polycrystalline as a-Si:H can be deposited at temperatures far below the nanowire growth temperature ensuring the cessation of silicon nanowire growth.

11.5 Conclusions
Silicon nanowires have been combined with amorphous silicon to form thin film devices. The nanowires, when coated in amorphous silicon layers were found to exhibit a coaxial morphology. The nanowires were found to have a high optical absorbance, which is a useful trait for a photovoltaic material to have as the power that is generated comes from the absorbed light. Silicon nanowires were observed to have photoconductive characteristics when left in their undoped state and when coated with p-type or n-type amorphous silicon. The source of the diode characteristics with intrinsic nanowires was likely due to the existence of Schottky diodes at the contacts to the nanowire films.

By using both n-type and p-type amorphous silicon layers, nanowire devices with strong diode characteristics that exhibited a photoconductive response were produced. Where the nanowires were embedded within an intrinsic amorphous silicon layer this effect was pronounced. Some devices of the Au-p-NW-i-n structure were found to have a demonstrable photovoltaic characteristic although only an extremely low efficiency was observed. This low efficiency was likely due to the migration of dopants within and from the amorphous p-layer during the high temperature nanowire growth phase. To overcome this problem a transverse
A prototype silicon nanowire based photovoltaic device was produced by using doped silicon nanowires as the p-layer. This device, although of low efficiency, had a demonstrable photocurrent. This indicates that thin film devices can be produced that incorporate silicon nanowires. With optimisation, the device would be expected to have higher efficiency and demonstrate the advantages of using silicon nanowires. These advantages include a high absorbance of light as shown in optical absorbance measurements, improved resistance to photodegradation due to the crystalline content and the ease and low cost of manufacture of thin film devices. The photocurrent shown by the devices using tin-catalysed doped silicon nanowires as a p-layer is encouraging and relevant for the use of these semiconductor nanostructures for photovoltaic applications.
Initially silicon nanowires were produced with a very low density. Only a few were to be found per sample. By altering and optimising the growth conditions, the density of the nanowires was increased. Silicon nanowires can be grown by a variety of methods. Three main deposition techniques used in this work were CVD, PECVD and PPECVD. Nanowires were successfully grown using CVD. However at low temperatures it was found that to ensure nanowire growth, a plasma was required. In Chapter 5 it was discussed that even for very long CVD durations nanowire growth did not occur yet the addition of only a few seconds of plasma time yielded good crops of silicon nanowires. A similar trend was observed at slightly higher temperatures where a pulsed plasma was used. In Chapter 9 it was shown that for the same period of CVD the addition of only a few seconds of PPECVD increased the coverage of silicon nanowires by 30% (Figure 9-6). The presence of a plasma improved the coverage of silicon nanowires in comparison to conventional CVD techniques. This has been previously observed by other groups in relation to PECVD (Hofmann et al., 2003, Colli et al., 2006). It was shown in Chapter 5 that the use of different durations of PECVD growth produced nanowires of similar lengths. From this it was proposed that the conditions for growth of silicon nanowires may be more favourable during the ignition or extinguishing phases of the plasma. As one can not turn the plasma on without tuning it off again to determine which of these phases was aiding the growth, the affect of having a larger proportion of these phases per deposition was investigated. That is, the plasma was pulsed with a square wave pulse with a range of frequencies. As was shown in Chapter 6, the use of a modulated plasma dramatically improved the density and sample coverage of silicon nanowires.
Chapter 12: Overall Discussions

PPECVD has been used in the deposition of amorphous silicon at high deposition rates without promoting dust formation (Das et al., 2003). Hence, it was expected that the use of PPECVD would improve the density of silicon nanowires and this was found to be the case. This improvement in nanowire density is likely to be more pronounced at temperatures near the lower end of the temperature range where nanowire growth occurs. The reasoning behind this is that the pulsed plasma is likely to aid substrate heating, assuring the catalyst droplets are liquid. For higher temperatures the effect may not be as pronounced. Due to this improvement in density, PPECVD was used as the preferred deposition method for producing silicon nanowires in this work. As far as the author is aware, this was the first time PPECVD has been used for the growth of silicon nanowires.

The first of the conditions to be optimised was substrate temperature. The maximum substrate temperature was limited by system specifications to ~345°C which is below the bulk eutectic point for gold and silicon. It was found that nanowire growth, using gold as a catalyst, could occur at these temperatures. It is well known that the melting point for nanoscale materials can be some few tens of degrees below the bulk melting point, or eutectic point in this case. For temperatures too far below the eutectic point, approximately 320°C, very few nanowires were grown. This was to be expected as the VLS mechanism by which these nanowires were grown requires the catalyst to be a liquid which, in the case of a gold silicon eutectic, occurs at 363°C for bulk materials and lower for nanoparticles.

The system pressure or the pressure of the reactant gasses also had an impact on the growth of the silicon nanowires. Initial trials with PECVD at different pressures showed that nanowire growth was denser at higher chamber pressures as discussed in Chapter 5. The result was found to be similar to that observed by other groups (Westwater et al., 1998) in that for higher pressures thinner nanowires were produced at a higher density than at low pressures. This was also in part resulting from increased substrate temperature at higher...
pressure due to the more efficient transport of heat from the heater block to the substrate via the reactant gases.

A trial, detailed in Chapter 9, involving the partial pressure of the main reactant gas (silane) was conducted for samples produced via PPECVD. It was found that the nanowires were produced with a higher coverage at higher partial pressures and that below a certain partial pressure few nanowires were produced. This was proposed to be due to the availability of sufficient silicon to completely form the eutectic. If insufficient silane was present, the correct ratios of gold and silicon would not have been present resulting in the catalyst not being liquid at the substrate temperature used. Interestingly it was found that the partial pressure used with PPECVD did not noticeably alter the diameter of the silicon nanowires for the range of pressures used and growth conditions that were used.

The most commonly used mechanism to produce silicon nanowires is the VLS mechanism with a metallic catalyst. The most preferred catalyst is gold, as it has a relatively low eutectic point with Si of 363°C, a variety of other catalysts such as titanium (Kamins et al., 2000), platinum, silver, palladium, copper and nickel (Wagner and Ellis, 1964) have also been used. Several different catalysts were trialled for their suitability to produce high density silicon nanowires under the temperature and pressure conditions available. The aim was to improve nanowire density and reduce material costs. It was found, as shown in Chapter 7, that of all the catalysts tested, tin and gold produced the highest coverage of nanowires. Other catalysts did produce silicon nanowires of differing morphologies and at a low coverage. The tin catalyst produced nanowires of a morphology distinctly different to those produced by gold catalysts. The tin-catalysed nanowires were of a thinner diameter and tended to bend and curve rather than kink. This could indicate an amorphous component. The particularly high density crops of thin nanowires produced by a tin catalyst were of interest as thin films of nanowires with a very even coverage could be produced. These films could then be used as
part of nanowire-based devices. To the author’s knowledge this was the first time thin films of Sn were used as a catalyst for the growth of silicon nanowires.

The diameter of the silicon nanowires produced in this thesis were systematically investigated in Chapter 5. This investigation was carried out by a controlled change in the thickness of the metal catalyst layer. The diameter of the silicon nanowire was found to be directly related to the thickness of the catalyst layer. This concurs with other results for gold catalysts, where it was found that nanowire diameter is determined by the diameter of the catalyst droplet (Cui et al., 2001). The size of the liquid catalyst droplet, when the sample is heated to the deposition temperature, is determined by the thickness of the catalyst layer deposited on the substrate (Wu et al., 2002).

Through the work in this thesis an effort was made to identify the variables influencing the nanowire diameter. The key influences on the diameter were identified as being the catalyst type discussed in Chapter 7, the catalyst layer thickness, investigated in Chapter 5 and the deposition type, explored in Chapter 9. The difference in diameter in this work and others is primarily due to the choice of catalyst, layer thickness and deposition conditions. It is well known and has been shown by Colli and co-workers (2006) that the use of PECVD tends to increase the nanowire diameter by the unwanted deposition of an amorphous silicon coating on the outside of the nanowire. The growth conditions in this thesis were optimised for areal density as it was deemed necessary that for a thin film device, a dense film of nanowires was preferable to scattered growth. The range of diameters of nanowires grown in this work is on the larger side of those reported in the literature (see Figure 2-9), but still of interest for photovoltaics. The average nanowire diameter in this work is actually smaller than some other studies on silicon nanowires for photovoltaics which used nanowires with diameters in the range of 200nm to 1500nm (Kelzenberg et al., 2008). Although quantum confinement occurs at lower diameters, as shown by the shift in crystalline silicon peak in Raman
spectroscopy, the use of crystalline materials rather than amorphous materials is of interest for other reasons. These include the improved absorption of light by a highly textured film (Hu and Chen, 2007, Peng et al., 2005) and the benefits of improved resistance to the Staebler-Wronski Effect by using crystalline materials in a thin film device.

The morphology of silicon nanowires is altered by the substrate upon which they are grown. A range of materials were used for the growth of silicon nanowires. It was found that the density of growth of the silicon nanowires was very dependent on substrate selection yet the diameter did not vary significantly between substrates. The growth alignment of the nanowires has been shown to be controllable by selection of the appropriate substrate crystal orientation. Gold-catalysed silicon nanowires in this work were grown on a variety of substrates including crystalline silicon of various orientations both HF-etched and with the native oxide left intact, polished stainless steel, polished copper, glass, ITO and amorphous silicon coated substrates.

As discussed in Chapter 8, very little in the way of oriented or aligned nanowire growth was observed on the crystalline silicon substrate, regardless of an HF etch before the coating with gold or before the sample was placed in the PPECVD chamber. This was probably due to the use of a relatively thick catalyst layer (~100nm) as opposed to the few nanometres used by other groups, the low substrate temperatures or the formation of an oxide layer after the HF etch and before the gold coating.

The metallic substrates would have been useful as back-contacts when producing photovoltaic devices. However, the stainless steel substrate only produced dense nanowires on some edge regions with only a few coiled wires present in the centre of the substrate. The copper substrates tended to grow platelet structures; yet in some regions did grow nanowires of a different morphology to the nanowires produced on crystalline silicon substrates. These
nanowires showed alignment, possibly growing epitaxially off of the platelet structures or from crystallites within the substrate. The exact mechanism behind this growth is unclear.

Silicon nanowires were grown on glass substrates, albeit with a low or intermittent coverage, using gold as a catalyst. It was shown that silicon nanowires could be grown with very high density on ITO-coated glass substrates of different glass thicknesses. This allows the nanowires to be grown in thin film structures on a solid transparent conducting substrate in order that photosensitive or photovoltaic devices can be produced. The variations in densities of nanowires between the different ITO coated glass samples used were due to the thickness of the glass and the correspondingly better contact to the heater block for thicker substrates. This is due to the design of the substrate holder but indicates that good thermal contact with the heater block is required so the substrates are at a high enough temperature for nanowire growth to occur.

Some glass and ITO substrates were coated with thick layers (~300nm) of amorphous silicon before being coated with a gold catalyst layer. It was found that nanowires would not grow reliably on these amorphous silicon coated substrates. This was possibly due to the presence of an insulating layer or the gold catalyst was being absorbed by the amorphous silicon and therefore unable to form the droplets required for VLS growth. This limits the types of structures that can be grown. However, it was noted that for the situation where a catalyst layer was deposited followed by a thin amorphous silicon layer before nanowire growth was triggered, the nanowires were able to grow through the layer. This was used to some advantage when producing the devices described in Chapter 11.

Doping of silicon nanowires is a useful step in creating silicon nanowire based devices as it allows the direct use of p-type and n-type nanowires. To determine if the doping was feasible on the deposition system being used, a number of experiments were conducted. The silane
gas used was undiluted whereas the diborane and phosphine were 1\% in argon. For the same
dopant ratios used for creating amorphous silicon devices, the partial pressure of silane in a
chamber at a total pressure of 3.0 torr would need to be less than 0.6 torr. To find out if
nanowires would grow in this partial pressure regime the silane was progressively diluted with
argon to the required pressure during deposition at several different silane flow rates. The
nanowires were found not to grow with a useable coverage below 1.5 torr for gold catalysts
and tin catalysts as was discussed in Chapter 9. The reduction in nanowire coverage at these
pressures was due in part to the temperatures used and the thickness of the catalyst layer
used. For thinner catalyst layers, the lower limit might be further reduced.

As the silicon nanowires could not be produced with dopant strength similar to that used in
doped amorphous silicon layers via \textit{in situ} doping, alternatives were pursued. Using intrinsic
silicon nanowires along with doped amorphous silicon n-layers and p-layers, devices were
fabricated as was shown in Chapter 11. The nanowires could be produced, however, with a
low dopant strength. These doped nanowires were used as a p-layer in a device also described
in Chapter 11.

Silicon nanowire films were combined with doped amorphous silicon layers to form
semiconductor devices with a number of configurations. It was shown in Chapter 11 that the
nanowire thin films would readily absorb visible light. The pristine, undoped nanowires were
found to show photoconductivity. That is, the conductivity of the nanowire films was shown
to increase with illumination. These two points alone indicate that silicon nanowires could
potentially form the basis of a photovoltaic device.

The silicon nanowire characteristics, as measured between an aluminium contact and an ITO
substrate, showed a distinct diode characteristic, or non-ohmic behaviour, as the result of
Schottky junctions occurring at the contact interfaces.
The nanowires were coated in doped amorphous silicon to change the diode characteristics. Embedding the nanowires inside an intrinsic amorphous silicon matrix tended to increase the photoconductivity change.

As mentioned above, gold-catalysed silicon nanowires would not grow readily on amorphous silicon coated substrates. The same result was observed when attempts were made to grow silicon nanowires on the top of an amorphous p-i-n device. That is, no nanowires grew on the device. In addition, the heat required for the growth actually destroyed the p-i-n junction, as evidenced by the photocurrent decaying to zero for the treated sample.

Where silicon nanowires were deposited before an amorphous p-i-n junction was deposited, it was found that the resistance in the sample was too great for a photocurrent to be evident. This was possibly a result of the fairly thick silicon nanowire layer.

One sample, with intrinsic silicon nanowires, that did show some photovoltaic response was an Au-p-NW-i-n device. This showed a very slight photoresponse, possibly inhibited by a relatively resistive NW layer, the migration of dopants from the p-layer during the nanowire deposition and internal shorting within the device. The shorting was likely a result from the random orientation of the silicon nanowires. However, internal shorting is not likely to be the major limiting factor. The silicon nanowires were found to have a coaxial morphology as shown in Figure 11-33. As such the nanowires were evenly coated in the various dopant layers as would have been the substrate, thus preventing internal shorts.

In addition to the layers of amorphous silicon, the nanowires were coated in aluminium. As discussed in Chapter 11, the nanowires were fairly evenly coated in aluminium. However the thickness of the aluminium layer on the wires was only obviously evident for extremely large aluminium thicknesses. The thick layers of aluminium tended to coat the silicon nanowires in
a spiked sheath. Although this could potentially contribute to internal shorts between the wires, it is unlikely, as the active semiconductor films were all evenly coated underneath the aluminium film.

To overcome the dopant migration from the p-layer during the high temperature phase of the silicon nanowire growth, a transverse design was trialled. This device did not show a photovoltaic effect within the sensitivity of the instrumentation used. However a weak diode effect was observed. This was due to the physical size of the device with the i-layer being greater than 3mm across.

A device was produced that used doped tin-catalysed silicon nanowires as a p-layer, amorphous silicon as an i-layer and amorphous silicon as an n-layer was produced. This device demonstrated a measurable photocurrent and was a functioning solar cell. As mentioned in Chapter 11, the efficiency of this device was low, likely a result of the weak doping and the poor electron transport out of the thick nanowire layer. In addition, there may be only a few nanowires contributing to the total current of the device. However, by increasing the dopant strength or using a layer of smaller diameter nanowires, the efficiency of this prototype device is likely to improve. Due to limitations of the system, specifically the low percentage of diborane in the dopant gas (1% in argon), the nanowires could not be produced with a dopant concentration similar to that used in amorphous silicon p-layers. At low silane partial pressures, the density of silicon nanowires is much reduced. This thin film device, although of low efficiency, demonstrates that photovoltaic devices can be produced using a combination of doped silicon nanowires and amorphous silicon layers.

The small photovoltaic effect observed in the thin film device using tin-catalysed p-type silicon nanowires indicates that silicon nanowires could be the basis of photovoltaic devices. The nanowires could be used as either a thin film as attempted here, or as individual
nanowire devices as recently shown by Tian and co-workers (2007). The silicon nanowire thin film solar cell created in this thesis had a very similar fill factor to that of the nanowire device produced by Tian and co-workers (2007) but had a higher open circuit voltage. Silicon nanowire films effectively absorbed visible light incident upon them and from visual inspection could be seen to be extremely textured and anti-reflective. The silicon nanowires, both undoped and coated in doped a-Si:H, showed a significant conductivity change when illuminated. The doped silicon nanowires also exhibited good diode characteristics as required for a photovoltaic device. The current major limitation is the difficulty of doping the nanowires effectively in-situ. The production of a thin film nanowire based photovoltaic device and the properties of the silicon nanowires examined indicate that silicon nanowires have a great deal of potential as a material for photovoltaic applications.
CHAPTER 13: CONCLUSIONS

13.1 Conclusions
Nanometre scale silicon nanowires have been produced using an existing PECVD system with only a few minor modifications. The simplicity of these modifications indicates that silicon nanowires can be produced on existing deposition systems provided some growth conditions are met.

It was demonstrated that silicon nanowires could be grown at substrate temperatures of 335°C using an existing CVD and PECVD system. The PECVD system was later modified to allow the use of PPECVD. These temperatures were not overly different from the temperatures used to grow the thin film amorphous semiconductors used in some photovoltaic devices.

The use of the plasma was found to trigger the growth of the silicon nanowires and increase the growth rate of the nanowires in comparison to conventional CVD. The nanowires were deposited via the VLS mechanism where temperature was a key parameter in the growth process. For growth to occur, it was found that the substrate temperature needed to be close to the eutectic point of the catalyst and silicon. This was to ensure the droplet was liquid. Higher temperatures were preferable to ensure nanowire growth. However, as was shown, the nanowires could be grown below this temperature.

The diameter of the nanowire when gold was used as a catalyst was found to increase for larger catalyst layer thicknesses. By using a PECVD approach to the growth of silicon nanowires, it was found that silicon nanowires of high aspect ratio with a controlled diameter
could be produced. Control of the deposition parameters allowed control of the nanowire morphology and growth density.

Several alternative catalysts to the gold commonly used for nanowire growth via the VLS mechanism were trialled. It was found that all of the silver, aluminium, gold, copper, indium and tin catalysts that were used produced some silicon nanowires. However, it was found that tin and gold were the most effective catalysts for the growth conditions used. Tin had not been previously reported in the literature as being used as a thin film catalyst for the growth of silicon nanowires. However, it showed great potential. The nanowires catalysed by tin were found to have an average diameter significantly less than that of the gold catalyst, yielding dense nanowire films. For high density growth of silicon nanowires by PPECVD via the VLS mechanism, tin and gold are the preferred catalysts.

The use of PPECVD with a silane plasma modulated at frequencies between 125Hz and 1000Hz improved the density of silicon nanowires produced at substrate temperatures near to the eutectic point of gold and silicon. PPECVD had not previously been shown in the literature to be useful for the growth of silicon nanowires. The use of a pulsed plasma allowed the increase in growth density and total sample coverage without measurably altering the nanowire diameter. The repeated striking and extinguishing of the plasma was proposed as a likely cause for the improvement in growth density. This was due to some heating of the substrate or more favourable transient conditions in the start-up or extinguishing phases of the plasma. For substrate temperatures near or below the eutectic point of gold and silicon, the use of a pulsed silane plasma improved the density and sample coverage of the silicon nanowires grown in this work. It was also found that even very short PPECVD plasma durations yielded high density nanowire growth.
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Several different orientations of crystalline silicon substrates were used for the growth of silicon nanowires. It was found that the silicon nanowires did not grow with any sign of aligned growth on the different orientations of crystalline silicon substrates that were used. This was in contradiction to what was stated in the literature and was probably due to the thickness of the gold catalyst layer, the low substrate temperature or the formation of an oxide layer after the HF etch and before the gold coating. As the conditions used were not identical to those in the literature, some variation in results was to be expected. The thickness of the catalyst layer was the most significant change. Hence, this is likely to be the cause of the lack of epitaxial growth. Aligned growth was observed for silicon nanowires grown on polished copper substrates. This alignment was likely due to epitaxial growth of the nanowires from crystallites within the substrate or the platelets themselves.

Silicon nanowires were grown with high density on ITO-coated aluminosilicate glass. This showed that high density films of silicon nanowires could be grown *in situ* on transparent substrates. This is useful as thin film solar cells are often produced on transparent ITO coated substrates. The presence and composition of the ITO may be assisting the growth of the silicon nanowires.

Thin film semiconducting devices often use aluminium for electrical contacts. Coating the nanowires with varying thicknesses of aluminium caused the average diameter of the nanowires to increase. This is consistent with the addition of material evenly around the nanowire. For larger film thicknesses the nanowires became coated in a spiked sheath of aluminium. This showed that aluminium could readily adhere to the surface of the silicon nanowires allowing electrical contacts to be made. The durability of the nanowire thin films was investigated. The films were found to be susceptible to mechanical abrasion and scratching which indicated some protection from accidental damage would be needed for
silicon nanowire based devices as they are inherently fragile. Care must also be taken when making electrical contact to the device.

It was shown that the coverage of silicon nanowires decreased with decreasing silane partial pressure. This indicated that the doping of silicon nanowires, at the dopant concentration used for the standard amorphous silicon p-layers and n-layers, would not be possible. However, weakly doped p-type silicon nanowires could be produced.

Silicon nanowires were combined with doped amorphous silicon thin films to create semiconductor devices. The nanowires were observed to be photoconductive. When combined with doped amorphous silicon films the nanowire devices were shown to have strong diode characteristics. When silicon nanowires were used as a p-layer, the devices were shown to be photovoltaic and had a measurable photocurrent.

A prototype photovoltaic device was produced that consisted of a doped tin-catalysed silicon nanowire p-layer, an amorphous silicon i-layer and an amorphous silicon n-layer. The low efficiency of this device was possibly a result of the resistive and thick nature of the silicon nanowire film. The weakly doped p-type nanowire layer is also a contributor to the performance of this device. This device is similar to the design used by Tian and co-workers (2007), which had a p-type silicon nanowire core with intrinsic and n-type polycrystalline silicon sheaths. The design used in this work had not previously been shown in the literature and consisted of a thin film of p-type silicon nanowires coated, or sheathed, in intrinsic and n-type amorphous silicon. As shown in Chapter 11, these nanowires also had a coaxial morphology. Although only a low efficiency was attained from this device, there were several factors which indicate that silicon nanowires may be a promising material for photovoltaic devices. The un-optimised silicon nanowire thin film photovoltaic device had a fill factor equivalent to a good amorphous silicon solar cell. The silicon nanowire films were found to
effectively absorb visible light and were highly anti-reflective. The silicon nanowires were also shown to have a strong photoconductive effect and good diode characteristics when combined with doped amorphous silicon thin films. Further optimisation of the device that used p-type silicon nanowires by increasing the dopant strength in the p-layer or using lower diameter nanowires would result in a more efficient photovoltaic device.

The production of a prototype solar cell using p-type silicon nanowires and the properties of the silicon nanowires examined indicated that they have great potential as a material for photovoltaic and optoelectronic applications.

### 13.2 Recommendations for Further Work

The following further work is recommended as a result of this research:

1) To optimise the prototype silicon nanowire based solar cell. This could be done in several ways. The reduction of the thickness of the nanowire film would be advantageous as it would improve electron transport. This could be achieved through using tin as a catalyst and/or reducing the average nanowire diameter and length. The control of the diameter may be achieved by reducing the thickness of the metal catalyst film. The dopant concentration within the p-type silicon nanowire could be increased. This could be achieved by modifying the deposition system for higher temperatures and higher total pressures. This would allow the dopant ratio to be increased. An alternative method using post-growth doping could allow a more strongly doped p-layer to be used. This method would involve growing the nanowires and then annealing in the dopant gas.

2) Individual silicon nanowires may demonstrate a photovoltaic effect when coated with doped amorphous thin films in a coaxial configuration. Measurements of the
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photocurrent in these individual nanowire devices would be useful as they would allow comparison between nanowires sheathed in amorphous silicon and those sheathed in polycrystalline silicon.

3) A transverse silicon nanowire device would eliminate the need to heat the doped amorphous silicon layers. A transverse device design would allow the placement of the silicon nanowires in the i-layer. The optimisation of such a device through accurate masking techniques and the reduction of the width of the junction to ~500nm may produce an efficient photovoltaic device.

4) The band-gap of silicon nanowires is known to be dependant on the diameter of the nanowire. XPS studies of silicon nanowires as a function of the nanowire diameter would yield useful information about the changes in bonding and the density of states with nanowire diameter.

5) Further work needs to be done on determining the exact cause of the improved silicon nanowire growth when PPECVD was used. It was unclear if this was due to transients in the plasma or induced heating in the substrate. This could be investigated by using in situ spectroscopy of the plasma and observing the differences at different modulation frequencies. In situ detailed measurements of the temperature at the surface of the substrate may also be required.

6) A study on the islanding behaviour of the various catalysts, specifically gold and tin, on the range of substrates used in Chapter 8 would be of interest. This may serve to explain some of the differences in the diameters and growth characteristics of the nanowires grown in this thesis compared with other work in the literature.
7) Of interest in this work was the high density of growth of silicon nanowires on ITO. It was noted in this work that the ITO produced by two different manufacturers produced nanowire thin films with different densities of growth. A study of different ITO, ATO or other conductive coatings should be undertaken to determine if the composition of the TCO has any influence on the growth of the silicon nanowires.

8) Related to the further work mentioned above, the silicon nanowires were found to grow with low density on amorphous silicon coated substrates. This limited the variety of device designs that could be investigated. It would be of interest to determine explicitly why this is the case. It was proposed in this thesis that a bulk gold-silicon eutectic was forming and limiting growth. This should be investigated further.


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